PULSE AND DIGITAL CIRCUITS

LECTURE NOTES

B.TECH
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UNIT – I

LINEAR WAVESHAPING

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High pass, low pass RC circuits, their response for sinusoidal, step, pulse, square and ramp inputs. RC network as differentiator and integrator, attenuators, its applications in CRO probe, RL and RLC circuits and their response for step input, Ringing circuit.

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A linear network is a network made up of linear elements only. A linear network can be described by linear differential equations. The principle of superposition and the principle of homogeneity hold good for linear networks. In pulse circuitry, there are a number of waveforms, which appear very frequently. The most important of these are sinusoidal, step, pulse, square wave, ramp, and exponential waveforms. The response of *RC, RL,* and *RLC* circuits to these signals is described in this chapter. Out of these signals, the sinusoidal signal has a unique characteristic that it preserves its shape when it is transmitted through a linear network, i.e. under steady state, the output will be a precise reproduction of the input sinusoidal signal. There will only be a change in the amplitude of the signal and there may be a phase shift between the input and the output waveforms. The influence of the circuit on the signal may then be completely specified by the ratio of the output to the input amplitude and by the phase angle between the output and the input. No other periodic waveform preserves its shape precisely when transmitted through a linear network, and in many cases the output signal may bear very little resemblance to the input signal.

The process whereby the form of a non-sinusoidal signal is altered by transmission through a linear network is called linear wave shaping.

THE LOW-PASS *RC* CIRCUIT

Figure 1.1 shows a low-pass *RC* circuit. A low-pass circuit is a circuit, which transmits only low-frequency signals and attenuates or stops high-frequency signals.

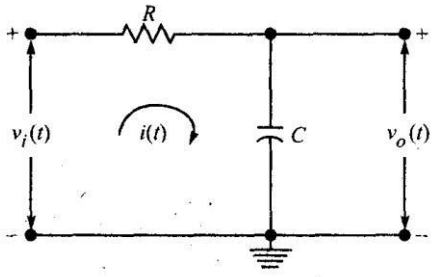


Figure 1.1 The low-pass *RC* circuit.

At zero frequency, the reactance of the capacitor is infinity (i.e. the capacitor acts as an open circuit) so the entire input appears at the output, i.e. the input is transmitted to the output with zero attenuation. So the output is the same as the input, i.e. the gain is unity. As the frequency increases the capacitive reactance decreases and so the output decreases. At very high frequencies the capacitor virtually acts as a short-circuit and the output falls to zero.

Sinusoidal Input

The Laplace transformed low-pass *RC* circuit is shown in Figure 1.2(a). The gain versus frequency curve of a low-pass circuit excited by a sinusoidal input is shown in Figure 1.2(b). This curve is obtained by keeping the amplitude of the input sinusoidal signal constant and varying its frequency and noting the output at each frequency. At low frequencies the output is equal to the input and hence the gain is unity. As the frequency increases, the output decreases and hence the gain decreases. The frequency at which the gain is $1/\sqrt{2}$ (= 0.707) of its maximum value is called the cut-off frequency. For a low-pass circuit, there is no lower cut-off frequency. It is zero itself. The upper cut-off frequency is the frequency (in the high-frequency range) at which the gain is $1/\sqrt{2}$. i-e- 70.7%, of its maximum value. The bandwidth of the low-pass circuit is equal to the upper cut-off frequency f_2 itself.

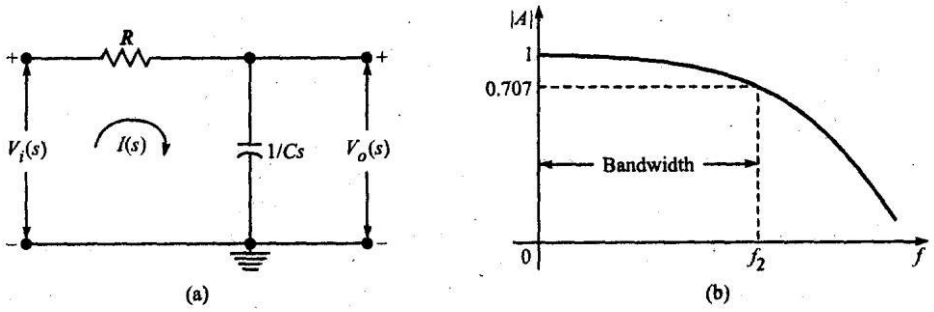


Figure 1.2 (a) Laplace transformed low-pass *RC* circuit and (b) its frequency response.

For the network shown in Figure 1.2(a), the magnitude of the steady-state gain A is given by

$$A = \frac{V_o(s)}{V_i(s)} = \frac{\frac{1}{Cs}}{R + \frac{1}{Cs}} = \frac{1}{1 + RCs} = \frac{1}{1 + j\omega RC} = \frac{1}{1 + j2\pi fRC}$$

$$\therefore \quad |A| = \frac{1}{\sqrt{1 + (2\pi fRC)^2}}$$

At the upper cut-off frequency f_2, $|A| = \frac{1}{\sqrt{2}}$

$$\therefore \quad \frac{1}{\sqrt{2}} = \frac{1}{\sqrt{1 + (2\pi f_2 RC)^2}}$$

Squaring both sides and equating the denominators,

$$2 = 1 + (2\pi f_2 RC)^2$$

$\therefore$ The upper cut-off frequency, $f_2 = \dfrac{1}{2\pi RC}$.

So $$A = \frac{1}{1 + j\dfrac{f}{f_2}} \quad \text{and} \quad |A| = \frac{1}{\sqrt{1 + \left(\dfrac{f}{f_2}\right)^2}}$$

The angle θ by which the output leads the input is given by

$$\theta = \tan^{-1} \frac{f}{f_2}$$

Step-Voltage Input

A step signal is one which maintains the value zero for all times $t < 0$, and maintains the value V for all times t > 0. The transition between the two voltage levels takes place at $t = 0$ and is accomplished in an arbitrarily small time interval. Thus, in Figure 1.3(a), $v_i = 0$ immediately before $t = 0$ (to be referred to as time $t = 0^-$) and $v_i = V$, immediately after t= 0 (to be referred to as time $t = 0^+$). In the low-pass *RC* circuit shown in Figure 1.1, if the capacitor is initially uncharged, when a step input is applied, since the voltage across the capacitor cannot change instantaneously, the output will be zero at $t = 0$, and then, as the capacitor charges, the output voltage rises exponentially towards the steady-state value V with a time constant *RC* as shown in Figure 1.3(b).

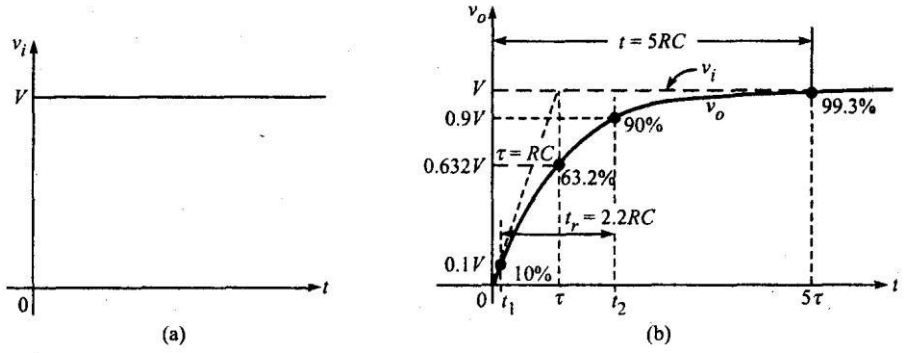


Figure 1.3 (a) Step input and (b) step response of the low-pass *RC* circuit.

Let V' be the initial voltage across the capacitor. Writine KVL around the IOOD in Fieure 1.1.

$$v_i(t) = Ri(t) + \frac{1}{C}\int i(t)\,dt$$

Differentiating this equation,

$$\frac{dv_i(t)}{dt} = R\,\frac{di(t)}{dt} + \frac{1}{C}i(t)$$

Since $v_i(t) = V, \quad \frac{dv_i(t)}{dt} = 0$

$$\therefore \quad 0 = R\frac{di(t)}{dt} + \frac{1}{C}i(t)$$

Taking the Laplace transform on both sides,

$$0 = R[sI(s) - I(0^+)] + \frac{1}{C}I(s)$$

$$\therefore \quad I(0^+) = I(s)\left(s + \frac{1}{RC}\right)$$

The initial current $I(0^+)$ is given by

$$I(0^+) = \frac{V - V'}{R}$$

$$\therefore \quad I(s) = \frac{I(0^+)}{s + \frac{1}{RC}} = \frac{V - V'}{R\left(s + \frac{1}{RC}\right)}$$

and $$V_o(s) = V_i(s) - I(s)R = \frac{V}{s} - \frac{(V - V')R}{R\left(s + \frac{1}{RC}\right)} = \frac{V}{s} - \frac{V - V'}{s + \frac{1}{RC}}$$

Taking the inverse Laplace transform on both sides,

$$v_o(t) = V - (V - V')e^{-t/RC}$$

where V' is the initial voltage across the capacitor (V_{initial}) and V is the final voltage (V_{final}) to which the capacitor can charge.

So, the expression for the voltage across the capacitor of an RC circuit excited by a step input is given by

$$v_o(t) = V_{\text{final}} - (V_{\text{final}} - V_{\text{initial}})e^{-t/RC}$$

If the capacitor is initially uncharged, then $v_o(t) = V(1 - e^{-t/RC})$

Expression for rise time

When a step signal is applied, the rise time t_r is defined as the time taken by the output voltage waveform to rise from 10% to 90% of its final value: It gives an indication of how fast the circuit can respond to a discontinuity in voltage. Assuming that the capacitor in Figure 1.1 is initially uncharged, the output voltage shown in Figure 1.3(b) at any instant of time is given by

$$v_o(t) = V(1 - e^{-t/RC})$$

At $t = t_1$, $v_o(t) \neq 10\%$ of $V = 0.1\,V$

$$\therefore \quad 0.1V = V(1 - e^{-t_1/RC})$$

$$\therefore \quad e^{-t_1/RC} = 0.9 \quad \text{or} \quad e^{t_1/RC} = \frac{1}{0.9} = 1.11$$

$$\therefore \quad t_1 = RC \ln (1.11) = 0.1RC$$

At $t = t_2$, $v_o(t) = 90\%$ of $V = 0.9\,V$

$$\therefore \quad 0.9V = V(1 - e^{-t_2/RC})$$

$$\therefore \quad e^{-t_2/RC} = 0.1 \quad \text{or} \quad e^{t_2/RC} = \frac{1}{0.1} = 10$$

$$\therefore \quad t_2 = RC \ln 10 = 2.3RC$$

$$\therefore \quad \text{Rise time, } t_r = t_2 - t_1 = 2.2RC$$

This indicates that the rise time t_r is proportional to the time constant RC of the circuit. The larger the time constant, the slower the capacitor charges, and the smaller the time constant, the faster the capacitor charges.

Relation between rise time and upper 3-dB frequency

We know that the upper 3-dB frequency (same as bandwidth) of a low-pass circuit is

$$f_2 = \frac{1}{2\pi RC} \quad \text{or} \quad RC = \frac{1}{2\pi f_2}$$

$$\therefore \quad \text{Rise time, } t_r = 2.2RC = \frac{2.2}{2\pi f_2} = \frac{0.35}{f_2} = \frac{0.35}{\text{BW}}$$

Thus, the rise time is inversely proportional to the upper 3-dB frequency.

The *time constant* (T= *RC)* of a circuit is defined as the time taken by the output to rise to 63.2% of the amplitude of the input step. It is same as the time taken by the output to rise to 100% of the amplitude of the input step, if the initial slope of rise is maintained. See Figure 1.3(b). The Greek letter T is also employed as the symbol for the time constant.

Pulse Input

The pulse shown in Figure 1.4(a) is equivalent to a positive step followed by a delayed negative step as shown in Figure 1 .4(b). So, the response of the low-pass *RC* circuit to a pulse for times less than the pulse width t_p is the same as that for a step input and is given by $v_0(t) = V(1 - e^{-t/RC})$. The responses of the low-pass *RC* circuit for time constant $RC \gg t_p$, *RC* smaller than t_p and *RC* very small compared to t_p are shown in Figures 1.5(a), 1.5(b), and 1.5(c) respectively.

If the time constant *RC* of the circuit is very large, at the end of the pulse, the output voltage will be $V_p(t) = V(1 - e^{-t_p/RC})$, and the output will decrease to zero from this value with a

time constant *RC* as shown in Figure 1.5(a). Observe that the pulse waveform is distorted when it is passed through a linear network. The output will always extend beyond the pulse width t_p, because whatever charge has accumulated across the capacitor *C* during the pulse cannot leak off instantaneously.

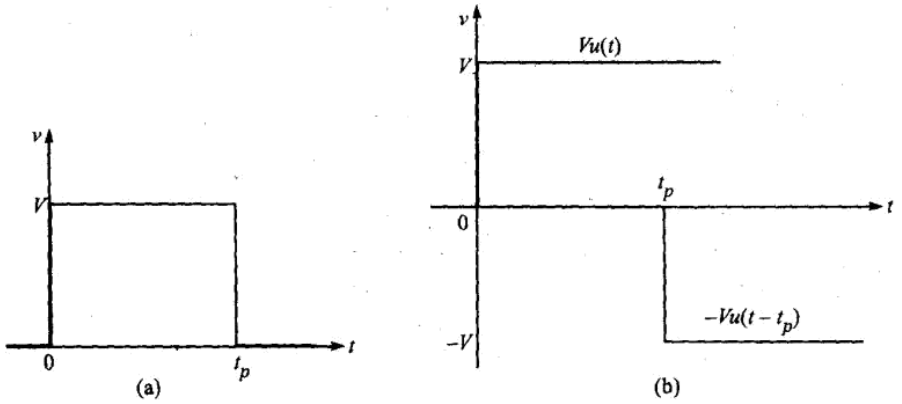


Figure 1.4 (a) A pulse and (b) a pulse in terms of steps.

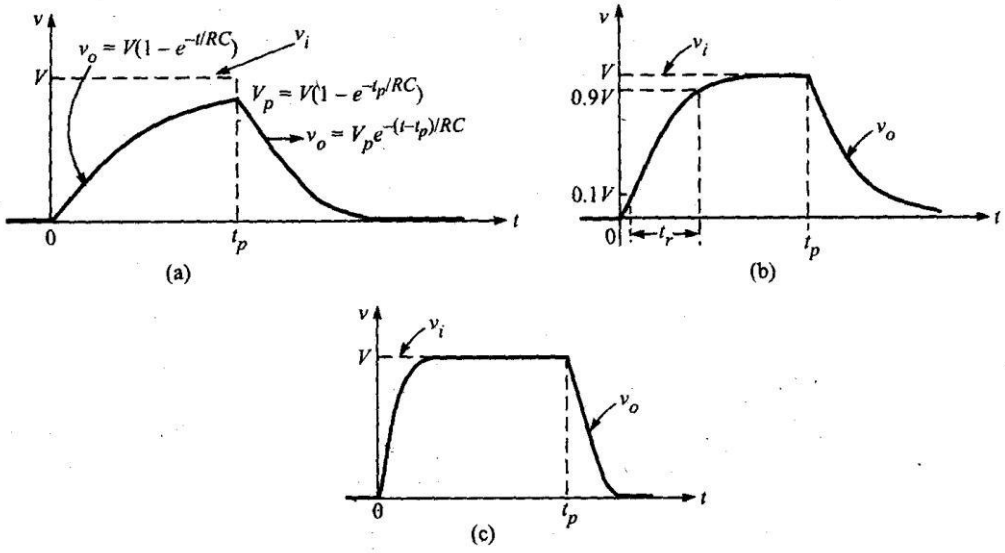


Figure 1.5 Pulse response for (a) $RC >> t_p$, (b) $RC < t_p$, and (c) $RC << t_p$.

If the time constant *RC* of the circuit is very small, the capacitor charges and discharges very quickly and the rise time t_r will be small and so the distortion in the wave shape is small. For minimum distortion (i.e. for preservation of wave shape), the rise time must be small compared to the pulse width t_p. If the upper 3-dB frequency $/_2$ is chosen equal to the reciprocal of the pulse width t_p, i.e. if $f_2 = 1/t_p$ then $t_r = 0.35t_p$ and the output is as shown in Figure 1.5(b), which for many applications is a reasonable reproduction of the input. As a rule of thumb, we can say:

A pulse shape will be preserved if the 3-dB frequency is approximately equal to the reciprocal of the pulse width.

Thus to pass a 0.25 μ.s pulse reasonably well requires a circuit with an upper cut-off frequency of the order of 4 MHz.

Square-Wave Input

A square wave is a periodic waveform which maintains itself at one constant level V' with respect to ground for a time T_1 and then changes abruptly to another level V'', and remains constant at that level for a time T_2, and repeats itself at regular intervals of $T = T_1 + T_2$. A square wave may be treated as a series of positive and negative steps. The shape of the output waveform for a square wave input depends on the time constant of the circuit. If the time constant is very small, the rise time will also be small and a reasonable reproduction of the input may be obtained.

For the square wave shown in Figure 1.6(a), the output waveform will be as shown in Figure 1.6(b) if the time constant RC of the circuit is small compared to the period of the input waveform. In this case, the wave shape is preserved. If the time constant is comparable with the period of the input square wave, the output will be as shown id Figure 1.6(c). The output rises and falls exponentially. If the time constant is very large compared to the period of the input waveform, the output consists of exponential sections, which are essentially linear as indicated in Figure 1.6(d). Since the average voltage across R is zero, the dc voltage at the output is the same as that of the input. This average value is indicated as $V\&$. in all the waveforms of Figure 1.6.

In Figure 1.6(c), the equation for the rising portion is

$$v_{01} = V' - (V' - V_2)e^{-t/RC}$$

where V_2 is the voltage across the capacitor at $t = 0$, and V' is the level to which the capacitor can charge.

The equation for the falling portion is

$$v_{02} = V'' - (V'' - V_1)e^{-(t - T_1)/RC}$$

where V_1 is the voltage across the capacitor at $t = T_1$ and V'' is the level to which the capacitor can discharge.

Setting $v_{01} = V_1$ at $t = T_1$,

$$V_1 = V' - (V' - V_2)e^{-T_1/RC} = V'(1 - e^{-T_1/RC}) + V_2e^{-T_1/RC}$$

Setting $v_{02} = V_2$ at $t = T_1 + T_2$,

$$V_2 = V'' - (V'' - V_1)e^{-(T_1+T_2-T_1)/RC} = V''(1 - e^{-T_2/RC}) + V_1e^{-T_2/RC}$$

Substituting this value of V_2 in the expression for V_1,

$$V_1 = V'(1 - e^{-T_1/RC}) + [V''(1 - e^{-T_2/RC}) + V_1 e^{-T_2/RC}]e^{-T_1/RC}$$

i.e.
$$V_1 = \frac{V'(1-e^{-T_1/RC}) + V''(1-e^{-T_2/RC})e^{-T_1/RC}}{1-e^{-(T_1+T_2)/RC}}$$

Similarly substituting the value of V_1 in the expression for V_2,

$$V_2 = \frac{V''(1 - e^{-T_2/RC}) + V'(1 - e^{-T_1/RC})\, e^{-T_2/RC}}{1 - e^{-(T_1+T_2)/RC}}$$

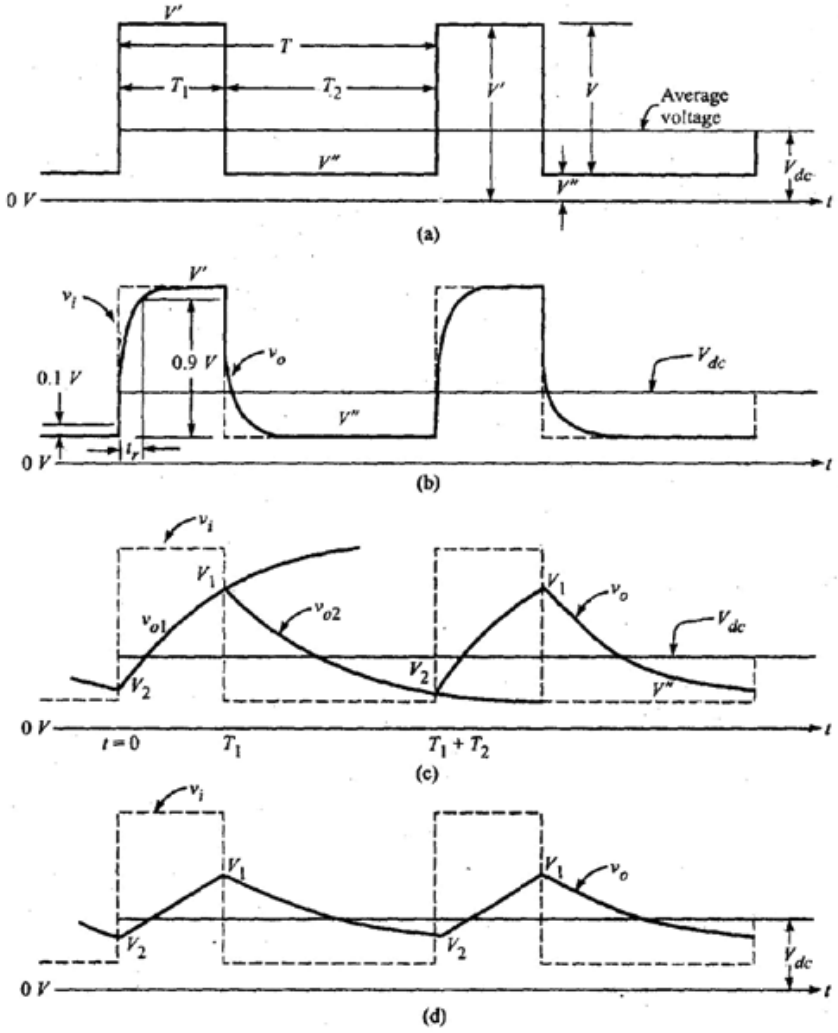


Figure 1.6 Response of a low-pass *RC* circuit to a square wave input: (a) square-wave input wave form, (b) output waveform for $RC \ll T$, (c) output waveform for $RC \approx T$, and (d) output waveform for $RC \gg T$.

For a symmetrical square wave with zero average value,

$T_1 = T_2 = \frac{T}{2}$ and $V' = -V'' = \frac{V}{2}$. So, V_2 will be equal to $-V_1$

$$\therefore \qquad V_1 = \frac{\frac{V}{2}(1 - e^{-T/2RC}) - \frac{V}{2}(1 - e^{-T/2RC})\, e^{-T/2RC}}{1 - e^{-T/RC}}$$

$$= \frac{V}{2} \frac{1 - e^{-T/2RC} - e^{-T/2RC} + e^{-T/RC}}{1 - e^{-T/RC}}$$

$$= \frac{V}{2} \frac{(1 - e^{-T/2RC})^2}{(1 + e^{-T/2RC})(1 - e^{-T/2RC})}$$

$$= \frac{V}{2} \left(\frac{1 - e^{-T/2RC}}{1 + e^{-T/2RC}} \right)$$

$$= \frac{V}{2} \left(\frac{e^{T/2RC} - 1}{e^{T/2RC} + 1} \right)$$

$$= \frac{V}{2} \left(\frac{e^{2x} - 1}{e^{2x} + 1} \right) = \frac{V}{2} \tanh x$$

where $x = \dfrac{T}{4RC}$ and T is the period of the square wave.

Now, $$V_2 = -V_1 = -\frac{V}{2}\left(\frac{1 - e^{-T/2RC}}{1 + e^{-T/2RC}} \right) = \frac{V}{2} \left(\frac{1 - e^{T/2RC}}{1 + e^{T/2RC}} \right)$$

1.1.5 Ramp Input

When a low-pass RC circuit shown in Figure 1.1 is excited by a ramp input, i.e.

$v_i(t) = \alpha t$, where α is the slope of the ramp

we have, $$V_i(s) = \frac{\alpha}{s^2}$$

From the frequency domain circuit of Figure 1.2(a), the output is given by

$$V_o(s) = V_i(s) \frac{\dfrac{1}{Cs}}{R + \dfrac{1}{Cs}} = \frac{\alpha}{s^2} \cdot \frac{1}{1 + RCs} = \frac{\alpha}{RC} \frac{1}{s^2\left(s + \dfrac{1}{RC} \right)}$$

$$= \frac{\alpha}{RC} \left[\frac{-(RC)^2}{s} + \frac{RC}{s^2} + \frac{(RC)^2}{s + \dfrac{1}{RC}} \right]$$

i.e. $$V_o(s) = \frac{-\alpha RC}{s} + \frac{\alpha}{s^2} + \frac{\alpha RC}{s + \dfrac{1}{RC}}$$

Taking the inverse Laplace transform on both sides,

$$v_o(t) = -\alpha RC + \alpha t + \alpha RCe^{-t/RC}$$
$$= \alpha(t - RC) + \alpha RCe^{-t/RC}$$

If the time constant RC is very small, $e^{-t/RC} \approx 0$

$$\therefore \quad v_o(t) = \alpha(t - RC)$$

When the time constant is very small relative to the total ramp time T, the ramp will be transmitted with minimum distortion. The output follows the input but is delayed by one time constant RC from the input (except near the origin where there is distortion) as shown in Figure 1.7(a). If the time constant is large compared with the sweep duration, i.e. if $RCIT \gg 1$, the output will be highly distorted as shown in Figure 1.7(b).

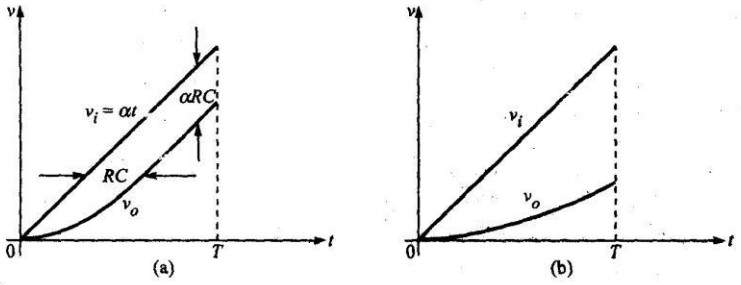


Figure 1.7 Response of a low-pass RC circuit for a ramp input for (a) $RC/T \ll 1$ and (b) $RC/T \gg 1$.

Expanding $e^{-t/RC}$ in to an infinite series in t/RC in the above equation for $v_o(t)$,

$$v_o(t) = \alpha(t - RC) + \alpha RC\left(1 - \frac{t}{RC} + \left(\frac{t}{RC}\right)^2 \frac{1}{2!} - \left(\frac{t}{RC}\right)^3 \frac{1}{3!} + \ldots\right)$$
$$= \alpha t - \alpha RC + \alpha RC - \alpha t + \frac{\alpha t^2}{2RC} - \ldots$$
$$\approx \frac{\alpha t^2}{2RC} \approx \frac{\alpha}{RC}\left(\frac{t^2}{2}\right)$$

This shows that a quadratic response is obtained for a linear input and hence the circuit acts as an integrator for $RC/T \gg 1$.

The transmission error e_t for a ramp input is defined as the difference between the input and the output divided by the input at the end of the ramp, i.e. at $t = T$.

For $RC/T \ll 1$,

$$e_t = \left.\frac{\alpha t - (\alpha t - \alpha RC)}{\alpha t}\right|_{t=T}$$
$$= \frac{\alpha RC}{\alpha T} = \frac{RC}{T} = \frac{1}{2\pi f_2 T}$$

where f_2 is the upper 3-dB frequency. For example, if we desire to pass a 2 ms pulse with less than 0.1% error, the above equation yields $f_2 > 80$ kHz and $RC < 2$ μ.s.

THE LOW-PASS *RC* CIRCUIT AS AN INTEGRATOR

If the time constant of an *RC* low-pass circuit is very large, the capacitor charges very slowly and so almost all the input voltage appears across the resistor for small values of time. Then, the current in the circuit is *vffylR* and the output signal across *C* is

$$v_o(t) = \frac{1}{C}\int i(t)\,dt = \frac{1}{C}\int \frac{v_i(t)}{R}\,dt = \frac{1}{RC}\int v_i(t)\,dt$$

Hence the output is the integral of the input, i.e. if $v_i(t) = \alpha t$, then

$$v_o(t) = \frac{\alpha t^2}{2RC}$$

As time increases, the voltage drop across *C* does not remain negligible compared with that across *R* and the output will not remain the integral of the input. The output will change from a quadratic to a linear function of time. ***If the time constant of an RC low-pass circuit is very large in comparison with the. time required for the input signal to make an appreciable change, the circuit acts as an integrator.*** A criterion for good integration in terms of steady-state analysis is as follows: The low-pass circuit acts as an integrator provided the time constant of the circuit $RC > 15T$, where *T* is the period of the input sine wave. When *RC > 15T,* the input sinusoid will be shifted at least by 89.4° (instead of the ideal 90° shift required for integration) when it is transmitted through the network.

An *RC* integrator converts a square wave into a triangular wave. Integrators are almost invariably preferred over differentiators in analog computer applications for the following reasons:

1. It is easier to stabilize an integrator than a differentiator because the gain of an integrator decreases with frequency whereas the gain of a differentiator increases with frequency.
2. An integrator is less sensitive to noise voltages than a differentiator because of its limited bandwidth.
3. The amplifier of a differentiator may overload if the input waveform changes very rapidly.
4. It is more convenient to introduce initial conditions in an integrator.

EXAMPLE 1.1 A pulse generator with an output resistance $R_S = 500\ \Omega$ is connected to an oscilloscope with an input capacitance of $C_i = 30$ pF. Determine the fastest rise time that can be displayed.

Solution: The circuit works as a low-pass filter shown in Figure 1.1 with a time constant

$$R_S C_i = 500\ \Omega \times 30\ \text{pF} = 15\ \text{ns}$$

$\therefore$ Fastest rise time, $t_r = 2.2RC = 2.2 \times 15\ \text{ns} = 33\ \text{ns}$

EXAMPLE 1.2 A 10 V step is switched on to a 50 kΩ resistor in series with a 500 pF capacitor. Calculate the rise time of the capacitor voltage, the time for the capacitor to charge to 63.2% of its maximum voltage, and the time for the capacitor to be completely charged.

Solution: The circuit acts as a low-pass filter shown in Figure 1.1.

(a) The rise time of the capacitor voltage is

$$t_r = 2.2RC = 2.2 \times 50\ \text{k}\Omega \times 500\ \text{pF} = 55\ \mu\text{s}$$

(b) The time for the capacitor to charge to 63.2% of the maximum voltage is

$$\tau = RC = 50\ \text{k}\Omega \times 500\ \text{pF} = 25\ \mu\text{s}$$

(c) The time for the capacitor to be completely charged (99% value) is

$$5\tau = 5RC = 5 \times 25\ \mu\text{s} = 125\ \mu\text{s}$$

THE HIGH-PASS *RC* CIRCUIT

Figure 1.30 shows a high-pass *RC* circuit. At zero frequency the reactance of the capacitor is infinity and so it blocks the input and hence the output is zero. Hence, this capacitor is called the *blocking capacitor* and this circuit, also called the *capacitive coupling circuit,* is used to provide dc isolation between the input and the output. As the frequency increases,'the reactance of the capacitor decreases and hence the output and gain increase. At very high frequencies, the capacitive reactance is very small so a very small voltage appears, across *C* and, so the output is almost equal to the input and the gain is equal to 1. Since this circuit attenuates low-frequency signals and allows transmission of high-frequency signals with little or no attenuation, it is called a high-pass circuit.

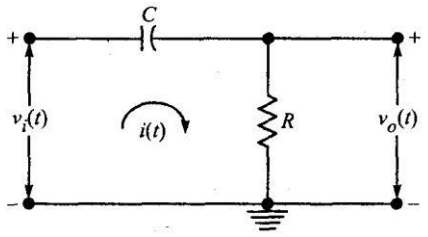


Figure 1.30 The high-pass *RC* circuit.

Sinusoidal Input

Figure 1.31 (a) shows the Laplace transformed high-pass *RC* circuit. The gain versus frequency curve of a high-pass circuit excited by a sinusoidal input is shown in Figure 1.31(b). For a sinusoidal input v,, t;he output signal v_0 increases in amplitude with increasing frequency. The frequency at which the gain is 1/V2 of its maximum value is called the lower cut-off or lower 3-dB frequency. For a high-pass circuit, there is no upper cut-off frequency because all high frequency signals are transmitted with zero attenuation. Therefore, $f_2 - f_1$. Hence bandwidth B.W= f_2 - fi =∞

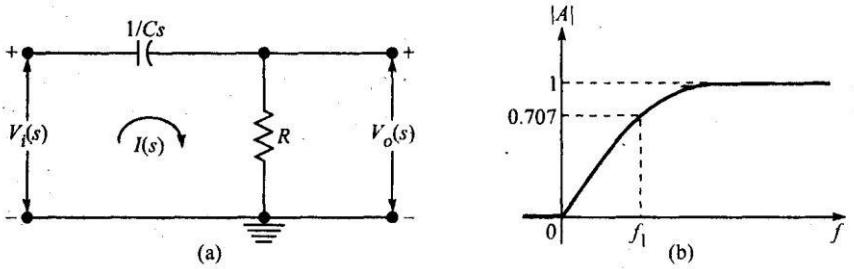


Figure 1.31 (a) Laplace transformed high-pass circuit and (b) gain versus frequency plot.

Expression for the lower cut-off frequency

For the high-pass *RC* circuit shown in Figure 1.31 (a), the magnitude of the steady-state gain *A*, and the angle θ by which the output leads the input are given by

$$A = \frac{V_o(s)}{V_i(s)} = \frac{R}{R + \frac{1}{Cs}} = \frac{1}{1 + \frac{1}{RCs}}$$

Putting $s = j\omega$, $A = \dfrac{1}{1 - j\frac{1}{\omega RC}} = \dfrac{1}{1 - j\frac{1}{2\pi fRC}}$

$\therefore$ $|A| = \dfrac{1}{\sqrt{1 + \left(\frac{1}{2\pi fRC}\right)^2}}$ and $\theta = -\tan^{-1}\dfrac{1}{2\pi fRC}$

At the lower cut-off frequency f_1, $|A| = 1/\sqrt{2}$

$\therefore$ $\dfrac{1}{\sqrt{1 + \left(\frac{1}{2\pi f_1 RC}\right)^2}} = \dfrac{1}{\sqrt{2}}$

Squaring and equating the denominators,

$$\frac{1}{2\pi f_1 RC} = 1 \quad \text{i.e.} \quad f_1 = \frac{1}{2\pi RC}$$

This is the expression for the lower cut-off frequency of a high-pass circuit.

Relation between f_1 and tilt

The lower cut-off frequency of a high-pass circuit is /i = *\/2nRC.* The lower cut-off frequency produces a tilt.For a 10% change in capacitor voltage, the time or pulse width involved is

$$t = 0.1RC = \text{PW}$$

$$\therefore \quad \frac{\text{PW}}{RC} = 0.1 = \text{Fractional tilt}$$

$$\therefore \quad \text{Fractional tilt} = \frac{\text{PW}}{RC} = 2\pi f_1 \cdot \text{PW}$$

This equation applies only when the tilt is 10% or less. When the tilt exceeds 10%, the voltage should be treated as exponential instead of linear and the equation $V_o = V_f - (V_f - V_i)e^{-t/RC}$ should be applied.

Step Input

When a step signal of amplitude *V* volts shown in Figure 1.32(a) is applied to the high-pass *RC* circuit of Figure 1.30, since the voltage across the capacitor cannot change instantaneously the output will be just equal to the input at $t = 0$ (for f < 0, v,- = 0 and $v_a = 0$). Later when the capacitor charges exponentially, the output reduces exponentially with the same time constant *RC.* The expression for the output voltage for $t > 0$ is given by

$v_o(t) = V_f - (V_f - V_{in})e^{-t/RC} = 0 - (0 - V)e^{-t/RC} = Ve^{-t/RC}$ Figure 1.32(b) shows the response of the circuit for large, small, and very small time constants.For $t > 5r$, the output will reach more than 99% of its final value. Hence although the steady state is approached asymptotically, for most applications we may assume that the final value has been reached after 5f. If the initial slope of the exponential is maintained, the output falls to zero in a time $t = T$.

The voltage across a capacitor can change instantaneously only when an infinite current passes through it, because for any finite current *i(t)* through the capacitor, the instantaneous change in voltage across the capacitor is given by $\frac{1}{C}\int_0^0 i(t)\,dt = 0$.

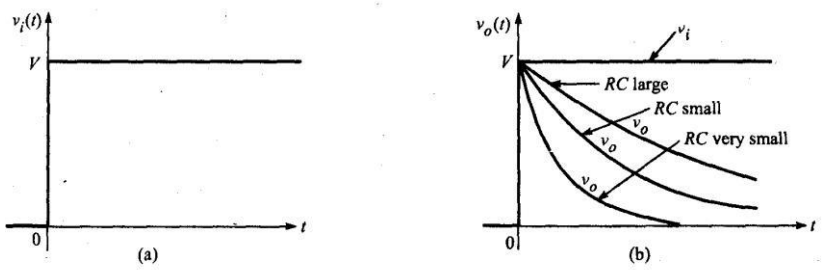


Figure 1.32 (a) Step input and (b) step response for different time constants.

Pulse Input

A pulse of amplitude V and duration t_p shown in Figure 1.4(a) is nothing but the sum of a positive step of amplitude V starting at $t = 0$ and a negative step of amplitude V starting at t_p as shown in Figure 1.4(b). So, the response of the circuit for $0 < t < t_,$, for the pulse input is the same as that for a step input and is given by $v_0(t) = Ve^{-t/RC}$. At $t = t_p$, $v_o(t) = V = Ve^{-t/RC}$. At $t = t_p$, since the input falls by V volts suddenly and since the voltage across the capacitor cannot change instantaneously, the output also falls suddenly by V volts to V_p - V. Hence at $t = t^+$, $v_a(t) = Ve^{-t_p/RC} - V$. Since $V_p < V$, $V_p - V$ is negative. So there is an undershoot at $t = t_p$ and hence for $t > t_p$, the output is negative. For $t > t_p$, the output rises exponentially towards zero with a time constant RC according to the expression $(Ve^{-t_p/RC} - V)e^{-(t-t_p)/RC}$.

The output waveforms for $RC \gg t_p$, RC comparable to t_p and $RC \ll t_p$ are shown in Figures 1.33(a), (b), and (c) respectively. There is distortion in the outputs and the distortion is the least when the time constant is very large. Observe that there is positive area and negative area in the output waveforms. The negative area will always be equal to the positive area. So if the time constant is very large the tilt (the almost linear decrease in the output voltage) will be small and hence the undershoot will be very small, and for $t > t_p$, the output rises towards the zero level very very slowly. If the time constant is very small compared to the pulse width (i.e. $RC/t_p \ll T$), the output consists of a positive spike or pip of amplitude V volts at the beginning of the pulse and a negative spike of the same amplitude at the end of the pulse. Hence a high-pass circuit with a very small time constant is called a *peaking circuit* and this process of converting pulses into pips by means of a circuit of short time constant is called peaking.

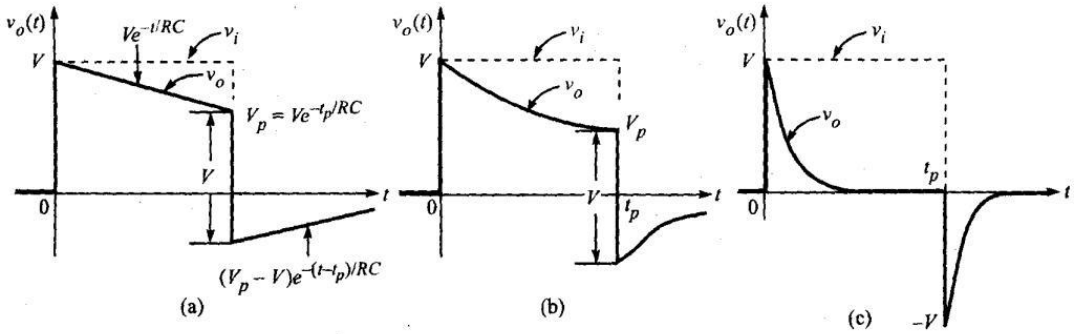


Figure 1.33 Pulse response for (a) $RC \gg t_p$, (b) RC comparable to t_p and (c) $RC \ll t_p$.

Square-Wave Input

A square wave shown in Figure 1.34(a) is a periodic waveform, which maintains itself at one constant level V with respect to ground for a time $T_{\{}$ and then changes abruptly to another level V'' and remains constant at that level for a time T_2, and then repeats itself at regular intervals of $T = T\backslash + T_2$. A square wave may be treated as a series of positive and negative steps. The shape of the output depends on the time constant of the circuit. Figures 1.34(b), 1.34(c), 1.34(d), and 1.34(e) show the output waveforms of the high-pass RC circuit under .steady-state conditions for the cases (a) $RC \gg T$, (b) $RC > T$, (c) $RC - T$, and (d) $RC \ll T$ respectively. When the time constant is arbitrarily large (i.e. RC/T_1 and RC/T_2 *are* very very large in comparison to unity) the output is same as the input but with zero dc level. When $RC > T$, the output is in the form of a tilt. When RC is comparable to T, the output rises and falls exponentially. When $RC \ll T$ (i.e. $RCIT\backslash$ and RC/T_2 *are very* small in comparison to unity), the output consists of alternate positive and negative spikes. In this case the peak-to-peak amplitude of the output is twice the peak-to-peak value of the input.In fact, for any periodic input waveform under steady-state conditions, the average level of the output waveform from the high-pass circuit of Figure 1.30 is always zero independently of the dc level of the input. The proof is as follows: Writing KVL around the loop of Figure 1.30,

$$v_i(t) = \frac{1}{C}\int i(t)\,dt + v_o(t)$$

$$= \frac{1}{RC}\int v_o(t)\,dt + v_o(t) \qquad \left(\because\ i(t) = \frac{v_o(t)}{R}\right)$$

Differentiating,

$$\frac{dv_i(t)}{dt} = \frac{v_o(t)}{RC} + \frac{dv_o(t)}{dt}$$

Multiplying by dt and integrating this equation over one period T,

$$\int_{t=0}^{t=T} dv_i(t) = \int_{t=0}^{t=T} \frac{v_o(t)\,dt}{RC} + \int_{t=0}^{t=T} dv_o(t)$$

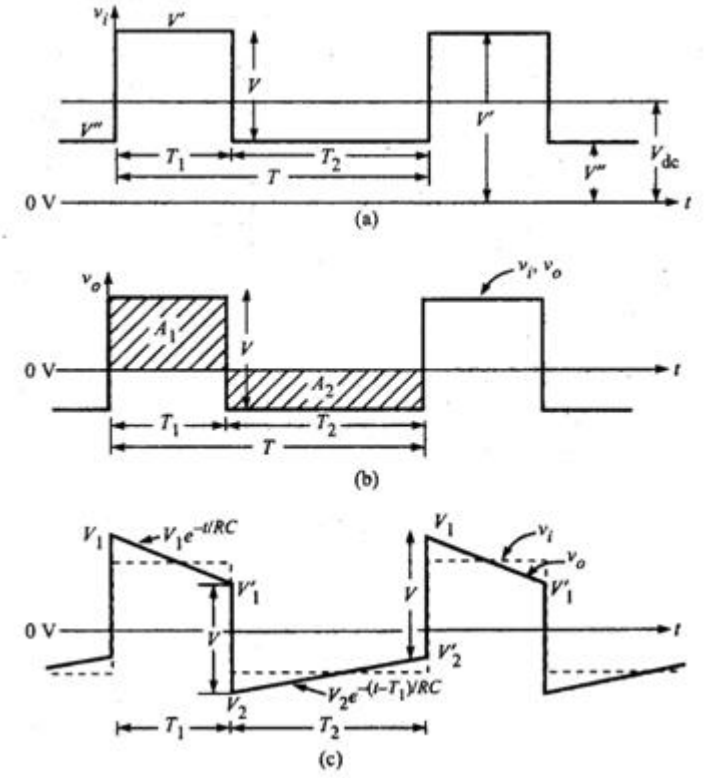
i.e. $$v_i(T) - v_i(0) = \frac{1}{RC}\int_0^T v_o(t)\,dt + v_o(T) - v_o(0)$$

Under steady-state conditions, the output waveform (as well as the input signal) is repetitive with a period T so that $v_o(T) = v_o(0)$ and $v_i(T) = v_i(0)$.

Under steady-state conditions, the output waveform (as well as the input signal) is repetitive with a period T so that $v_0(T) = v_0(0)$ and $v,(T) = v,(0)$.

Hence $\int_0^T v_o(t)\,dt = 0.$ Since this integral represents the area under the output waveform over one cycle, we can say that the average level of the steady-state output signal is always zero.This can also be proved based on frequency domain analysis as follows.The periodic input signal may be resolved into a Fourier series consisting of a constant term and an infinite number of sinusoidal components whose frequencies are multiples of / = 1/T. Since the blocking capacitor presents infinite impedance to the dc input voltage, none of these dc components reach the output under steady-state conditions. Hence the output signal is a sum of sinusoids whose frequencies are multiples of/. This waveform is therefore periodic with a fundamental period *T* but without a dc component.With respect to the high-pass circuit of Figure 1.30, we can say that:

1. The average level of the output signal is always zero, .independently of the average level of the input. The output must consequently extend in both negative and positive directions with respect to the zero voltage axis and the area of the part of the waveform above the zero axis must equal the area which is below the zero axis.
2. When the input changes abruptly by an amount *V*, the output also changes abruptly by an equal amount and in the same direction.
3. During any finite time interval when the input maintains a constant level, the output decays exponentially towards zero voltage.



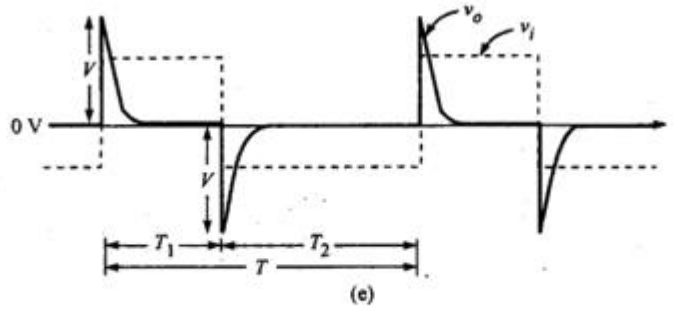


Figure 1.34 (a) A square wave input, (b) output when RC is arbitrarily large, (c) output when $RC > T$, (d) output when RC is comparable to T, and (e) output when $RC << T$.

Under steady-state conditions, the capacitor charges and discharges to the same voltage levels in each cycle. So the shape of the output waveform is fixed.

For $0 < t < T_1$, the output is given by $v_{o1} = V_1 e^{-t/RC}$

At $t = T_1$, $v_{o1} = V_1' = V_1 e^{-T_1/RC}$

For $T_1 < t < T_1 + T_2$, the output is $v_{o2} = V_2 e^{-(t-T_1)/RC}$

At $t = T_1 + T_2$, $v_{o2} = V_2' = V_2 e^{-T_2/RC}$

Also $V_1' - V_2 = V$ and $V_1 - V_2' = V$

From these relations V_1, V_1', V_2 and V_2' can be computed.

Expression for the percentage tilt

We will derive an expression for the percentage tilt when the time constant RC of the circuit is very large compared to the period of the input waveform, i.e. $RC » T$. For a symmetrical square wave with zero average value

$$V_1 = -V_2, \text{ i.e. } V_1 = |V_2|, \; V_1' = -V_2', \text{ i.e. } V_1' = |V_2'|, \text{ and } T_1 = T_2 = \frac{T}{2}$$

The output waveform for $RC >> T$ is shown in Figure 1.35. Here,

$$V_1' = V_1 e^{-T/2RC} \quad \text{and} \quad V_2' = V_2 e^{-T/2RC}$$

$$V_1 - V_2' = V$$

i.e. $$V_1 - V_2 e^{-T/2RC} = V_1 + V_1 e^{-T/2RC} = V$$

$\therefore$ $$V_1 = \frac{V}{1 + e^{-T/2RC}} \quad \text{or} \quad V = V_1(1 + e^{-T/2RC})$$

$$\% \text{ tilt, } P = \frac{V_1 - V_1'}{\frac{V}{2}} \times 100\% = \frac{V_1 - V_1 e^{-T/2RC}}{V_1(1 + e^{-T/2RC})} \times 200\% = \frac{1 - e^{-T/2RC}}{1 + e^{-T/2RC}} \times 200\%$$

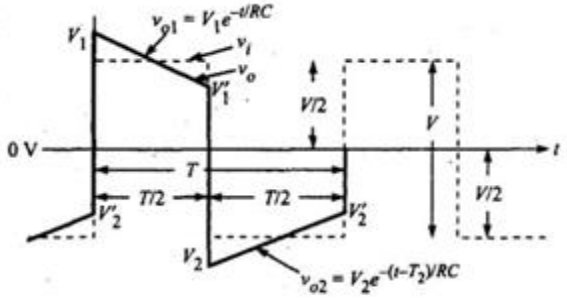


Figure 1.35 Linear tilt of a symmetrical square wave when $RC >> T$.

When the time constant is very large, i.e. $\frac{T}{RC} << 1$

$$P = \frac{1-\left[1+\left(\frac{-T}{2RC}\right)+\left(\frac{-T}{2RC}\right)^2\frac{1}{2!}+\ldots\right]}{1+1+\left(\frac{-T}{2RC}\right)+\left(\frac{-T}{2RC}\right)^2\frac{1}{2!}+\ldots} \times 200\%$$

$$= \frac{\frac{T}{2RC}}{2} \times 200\%$$

$$= \frac{T}{2RC} \times 100\%$$

$$= \frac{\pi f_1}{f} \times 100\%$$

where $f_1 = \frac{1}{2\pi RC}$ is the lower cut-off frequency of the high-pass circuit.

Ramp Input

A waveform which is zero for $t < 0$ and which increases linearly with time for / > 0 is called a ramp or sweep voltage.

When the high-pass *RC* circuit of Figure 1.30 is excited by a ramp input v/(r) = *at*, where *a* is the slope of the ramp, then

$$V_i(s) = \frac{\alpha}{s^2}$$

From the Laplace transformed circuit of Figure 1.31(a),

$$V_o(s) = V_i(s)\frac{R}{R+\frac{1}{Cs}} = \frac{\alpha}{s^2}\frac{RCs}{1+RCs}$$

$$= \frac{\alpha}{s\left(s+\frac{1}{RC}\right)} = \alpha RC\left(\frac{1}{s}-\frac{1}{s+\frac{1}{RC}}\right)$$

Taking the inverse Laplace transform on both sides,

$$v_o(t) = \alpha RC(1 - e^{-t/RC})$$

For times t which are very small in comparison with RC, we have

$$v_o(t) = \alpha RC\left[1-\left\{1+\left(\frac{-t}{RC}\right)+\left(\frac{-t}{RC}\right)^2\frac{1}{2!}+\left(\frac{-t}{RC}\right)^3\frac{1}{3!}+\ldots\right\}\right]$$

$$= \alpha RC\left[\frac{t}{RC}-\frac{t^2}{2(RC)^2}+\ldots\right]$$

$$= \alpha t-\frac{\alpha t^2}{2RC}=\alpha t\left(1-\frac{t}{2RC}\right)$$

Figure 1.36 shows the response of the high-pass circuit for a ramp input when (a) *RC» T,* and (b) *RC « T,* where *T* is the duration of the ramp. For small values of T, the output signal falls away slightly from the input as shown in the Figure 1.36(a).

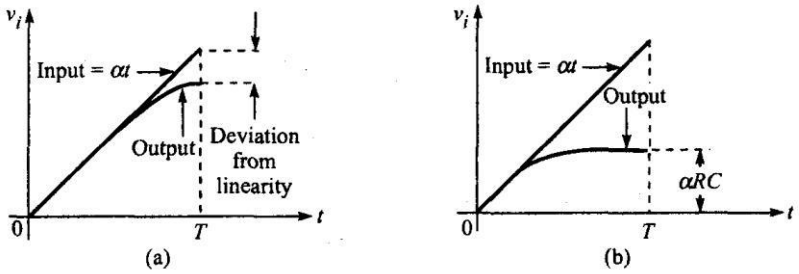


Figure 1.36 Response of the high-pass circuit for a ramp input when (a) $RC >> T$ and (b) $RC << T$.

When a ramp signal is transmitted through a linear network, the output departs from the input. A measure of the departure from linearity expressed as the transmission error *e,* is defined as the difference between the input and the output divided by the input. The transmission error at a time

$$e_t = \left.\frac{v_i - v_o}{v_i}\right|_{t=T} \approx \left.\frac{\alpha t-\alpha t\left(1-\frac{t}{2RC}\right)}{\alpha t}\right|_{t=T} \approx \frac{T}{2RC} = \pi f_1 T$$

where $f_1 = \dfrac{1}{2\pi RC}$ is the lower 3-dB frequency of the high-pass circuit.

$t = T$ is then

For large values of t in comparison with RC, the output approaches the constant value aRC as indicated in Figure 1.36(b).

THE HIGH-PASS *RC* CIRCUIT AS A DIFFERENTIATOR

When the time constant of the high-pass RC circuit is very very small, the capacitor charges very quickly; so almost all the input v,(0 appears across the capacitor and the voltage across the resistor will be negligible compared to the voltage across the capacitor. Hence the current is determined entirely by the capacit nce. Then the current

$$i(t) = C\frac{dv_i(t)}{dt}$$

and the output signal across R is

$$v_o(t) = RC\frac{dv_i(t)}{dt}$$

Thus we see that the output is proportional to the derivative of the input. ***The high-pass RC circuit acts as a differentiator provided the RC time, constant of the circuit is very small in comparison with the time required for the input signal to make an appreciable change.*** The

derivative of a step signal is an impulse of infinite amplitude at the occurrence of the discontinuity of step. The derivative of an ideal pulse is a positive impulse followed by a delayed negative impulse, each of infinite amplitude and occurring at the points of discontinuity. The derivative of a square wave is a waveform which is uniformly zero except, at the points of discontinuity. At these points, precise differentiation would yield impulses of infinite amplitude, zero width and alternating polarity. For a square wave input, an *RC* high-pass circuit with very small time constant will produce an output, which is zero except at the points of discontinuity. At these points of discontinuity, there will be peaks of finite amplitude *V.* This is because the voltage across *R* is not negligible compared with that across *C.*An *RC* differentiator converts a triangular wave into a square wave.For the ramp $v_i = at$, the value of $RC(dv/dt) = aRC$. This is true except near the origin. The output approaches the proper derivative value only after a lapse of time corresponding to several time constants. The error near $\theta = 0$ is again due to the fact that in this region the voltage across *R* is not negligible compared with that across *C.*

If we assume that the leading edge of a pulse can be approximated by a ramp, then we can measure the rate of rise of the pulse by using a differentiator. The peak output is measured on an oscilloscope, and from the equation = *aRC,* we see that this voltage divided by the product *RC* gives the slope *a.A criteria for good differentiation in terms of steady-state sinusoidal analysis is,* that if a sine wave is applied to the high-pass *RC* circuit, the output will be a sine

$$\tan\theta = \frac{X_C}{R} = \frac{1}{\omega RC}$$

wave shifted by a leading angle θ such that: with the output being proportional to $\sin(a>t + \theta)$. In order to have true differentiation, we must obtain cos ωt. In other words,θ must equal 90°. This result can be obtained only if R =,0 or C = 0.

However, if ωRC =0.01, then $1/\omega RC$ = 100 and θ = 89.4°, which is sufficiently close to 90° for most purposes. If ωRC = 0.1, then *90* - 84.3° and for some applications this may be close enough

to 90°.If the peak value of input is V_m, the output is and if $\omega RC \ll 1$, then the output is approximately $V_m \omega RC$ cos *(at.* This result agrees with the expected value $RC(dv_t/dt)$. If ωRC = 0.01, then the output amplitude is 0.01 times the input amplitude.

$$v_o = \frac{V_m R}{\sqrt{R^2 + \frac{1}{\omega^2 C^2}}} \sin(\omega t + \theta)$$

ATTENUATORS

Attenuators are resistive networks, which are used to reduce the amplitude of the input signal. The simple resistor combination of Figure 1.61 (a) would multiply the input signal by the ratio $a = R_2/(R_1 + R_2)$ independently of the frequency. If the output of the attenuator is feeding a stage of amplification, the input capacitance C_2 of the amplifier will be the stray capacitance shunting the resistor R_2 of the attenuator and the attenuator will be as shown in Figure 1.61(b), and the attenuation now is not independent of frequency. Using Thevenin's theorem, the circuit in Figure 1.61(b) may be replaced by its equivalent circuit shown in Figure 1,6l(c), in which R is equal to the parallel combination of R_1 and R_2.

Normally R_1 and R_2 must be large so that the nominal input impendence of the attenuator is large enough to prevent loading down the input signal. But if R_1 and R_2 are large, the rise time $t_r = 2.2[(R_1||R_2)*C_2]$ will be large and a large rise time is normally unacceptable.
The attenuator may be compensated by shunting R\ by a capacitor C\ as shown in Figure 1.61(d), so that its attenuation is once again independent of frequency. The circuit has been drawn in Figure 1.61(e) to suggest that the two resistors and the two capacitors may be viewed as the four arms of a bridge. If $R_1C_1 = R_2C_2$, the bridge will be balanced and no current will flow in the branch connecting the point X to the point Y. For the purpose of computing the output, the branch X-Y may be omitted and the output will again be equal to C_M, independent of the frequency. In practice, C_1 will ordinarily have to be made adjustable.
Suppose a step signal of amplitude V volts is applied to the circuit. As the input changes abruptly by V volts at t = 0, the voltages across Ci and C_2 will also change abruptly. This happens because at / = 0, the capacitors act as short-circuits and a very large (ideally infinite) current flows though the capacitors for an irifinitesimally small time so that a finite charge $q = \int_{0-}^{0+} i(t)\,dt$ is delivered to each capacitor. The initial output voltage is determined by the capacitors.

Since the same current flows through the capacitors C_1 and C_2, we have

$$\text{Charge accumulated in capacitor } C_1 = \int_{0^-}^{0^+} i(t)\,dt = q$$

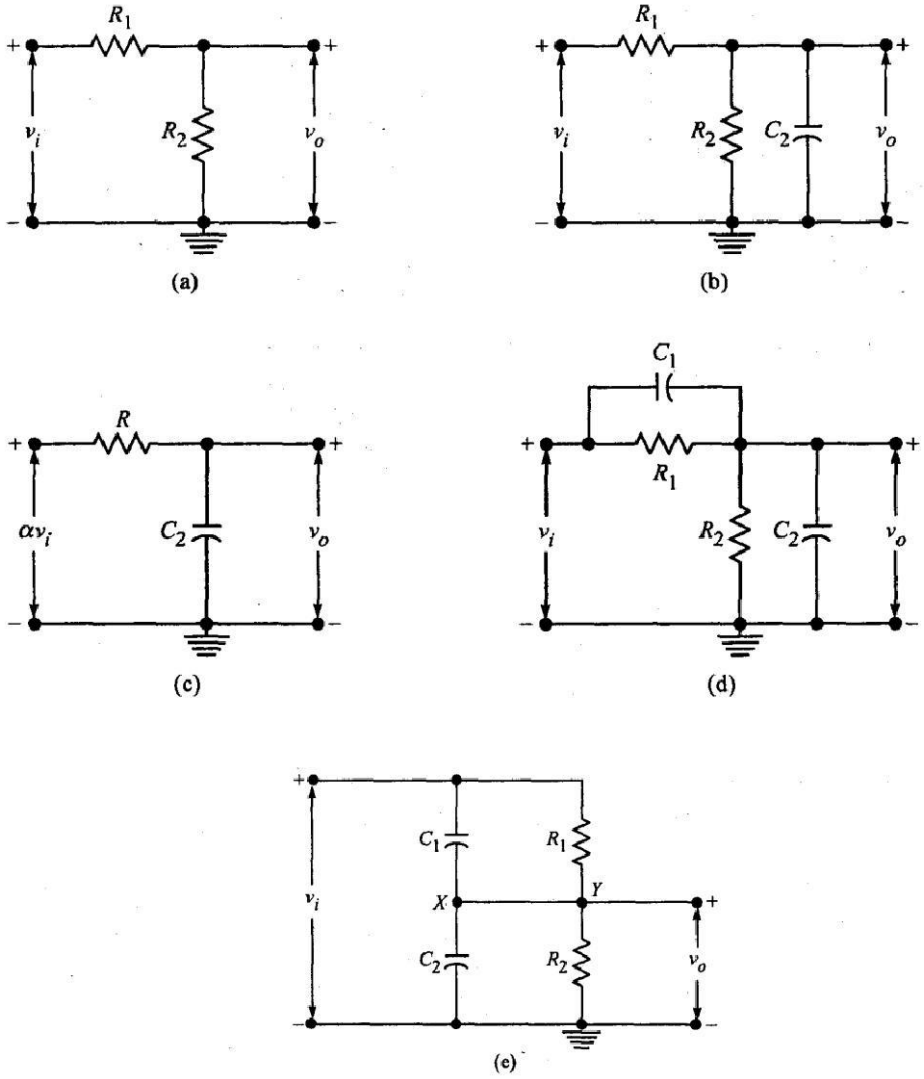


Figure 1.61 An attenuator: (a) ideal circuit, (b) actual circuit, (c) equivalent circuit, (d) compensated attenuator, and (e) compensated attenuator redrawn as a bridge.

$$\therefore \qquad \text{Initial voltage across } C_1 = \frac{q}{C_1} = V_1$$

Charge accumulated in capacitor $C_2 = \int_{0^-}^{0^+} i(t)\,dt = q$

Initial voltage across $C_2 = \frac{q}{C_2} = V_2 = v_o(0^+)$

Input signal, $V = V_1 + V_2 = \frac{q}{C_1} + \frac{q}{C_2} = q\left(\frac{C_1 + C_2}{C_1 C_2}\right)$

$$\frac{v_o(0^+)}{V} = \frac{\frac{q}{C_2}}{q\left(\frac{C_1 + C_2}{C_1 C_2}\right)} = \frac{C_1}{C_1 + C_2}$$

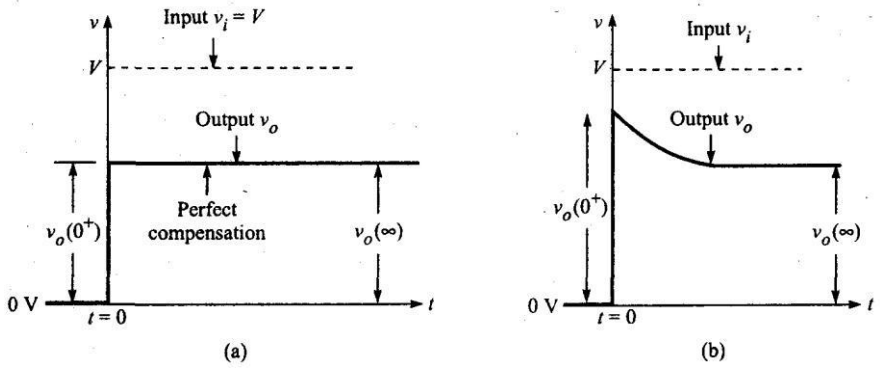
Or

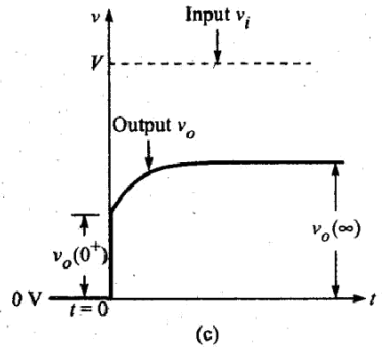
$$v_o(0^+) = V\frac{C_1}{C_1 + C_2} = v_i\frac{C_1}{C_1 + C_2}$$

The final output voltage is determined by the resistors *R*\ and R_2, because the capacitors C[and C_2 act as open circuits for the applied dc voltage under steady-state conditions. Hence

$$v_o(\infty) = V\frac{R_2}{R_1 + R_2} = v_i\frac{R_2}{R_1 + R_2}$$

Looking back from the output terminals (with the input short circuited) we see a resistor $R = R_{\{}R_2/(Ri + R_2)$ in parallel with C = $C_1 + C_2$. Hence the decay or rise of the output (when the attenuator is not perfectly compensated) from the initial to the final value takes place exponentially with a time constant $r = RC$. The responses of an attenuator for Cj equal to, greater than, and less than $R_2C_2/R_{\{}$ are indicated in Figure 1.62.





(a) perfect compensation means
$v_o(0^+) = v_o(\infty)$; $\therefore C_1 = \frac{R_2C_2}{R_1}$ i.e. $R_1C_1 = R_2C_2$
(b) over compensation means
$v_o(0^+) > v_o(\infty)$; $\therefore C_1 > R_2C_2/R_1$
(c) under compensation means
$v_o(0^+) < v_o(\infty)$; $\therefore C_1 < R_2C_2/R_1$

Figure 1.62 Response of compensated attenuator: (a) perfect compensation, (b) over compensation, and (c) under compensation.

Perfect compensation is obtained if $v_o(0^+) = v_o(\infty)$, that is, if the rise time $t_r = 0$

$$\therefore \quad V\frac{C_1}{C_1 + C_2} = V\frac{R_2}{R_1 + R_2}$$

i.e. $$R_1C_1 + R_2C_1 = R_2C_1 + R_2C_2$$

i.e. $$R_1C_1 = R_2C_2 \quad \text{or} \quad C_1 = \frac{R_2C_2}{R_1}$$

This is the balanced bridge condition. The extreme values of $v_0(0^+)$ are 0 for $C_1 = 0$ In the.above analysis we have assumed that an infinite current flows through the capacitors at $t = 0^+$ and hence the capacitors get charged instantaneously. This is valid only if the generator resistance is zero. In general, the output resistance of the generator is not zero but is of some finite value. Hence the impulse response is physically impossible. So, even though the attenuator is compensated, the ideal step response can never be obtained. Neverthless, an improvement in rise time does result if a compensated attenuator is used. For example, if the output is one-tenth of the input, then the rise time of the output using the attenuator is one-tenth of what it would be without the attenuator.

The compensated attenuator will reproduce faithfully the signal, which appears at its input terminals. However, if the output impedance of the generator driving the attenuator is not zero, the signal will be distorted right at the input to the attenuator. This situation is illustrated in Figure 1.63(a) in which a generator of step voltage V and of source resistance R_S is connected to the attenuator. Since the lead which joins the point X and point Y may be open circuited, the circuit may be redrawn as in Figure 1.63(b). Usually R_S « R_1+ R_2, so the input to the attenuator will be an exponential of time constant RsC', where C' is the capacitance of the series combination of Cj and C_2> i.e. $C' = C_1\ C/(C_1 + C_2)$. It is this exponential waveform rather than the step, which the attenuator will transmit faithfully. If the generator terminals were

connected directly to the terminals to which the attenuator output is connected, the generator would see a capacitance C_2. In this case the waveform at these terminals would be an exponential with time constant T = RsC_2.

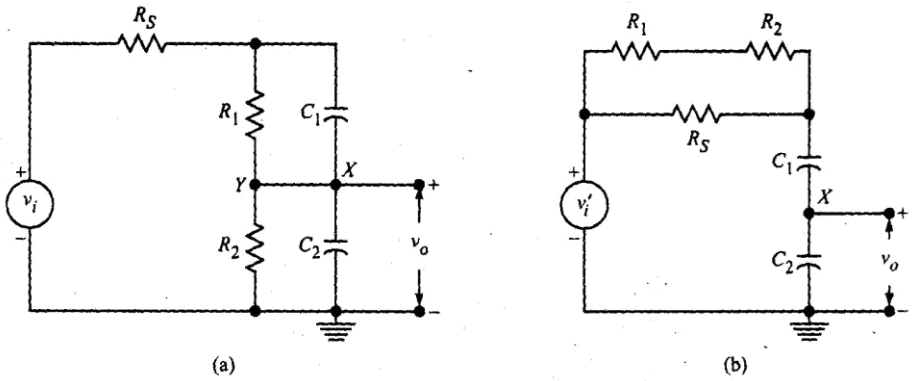


Figure 1.63 (a) Compensated attenuator including source resistance R_S and (b) its equivalent circuit with $v_i' = V(R_1 + R_2)/(R_S + R_1 + R_2)$.

When the attenuator is used^ the time constant is T' = $R\$C^f$. $\frac{\tau'}{\tau} = \frac{C'}{C_2} = \frac{C_1}{C_1 + C_2} = a$ an improvement in waveform results. For example, if the attenuation is equal to 10(a = 1/10), then the rise time of the waveform would be divided by a factor 10.-

RL CIRCUITS

In previous session we discussed the behaviour of *RC* low-pass and high-pass circuits for various types of input waveforms. Suppose the capacitor *C* and-resistor *R* in those circuits are replaced by a resistor *R'* and an inductor *L* respectively, then, if the time constant *LIR'* equals the time constant *RC,* all the preceding results remain unchanged.

When a large time constant is required, the inductor is rarely used because a large value of inductance can be obtained only with an iron-core inductor which is physically large, heavy and expensive relative to the cost of a capacitor for a similar application. Such an iron-cored inductor will be shunted with a large amount of stray distributed capacitance. Also the nonlinear properties of the iron cause distortion, which may be undesirable. If it is required to pass very low frequencies through a circuit in which *L* is" a shunt element, then the inductor may become prohibitively large. Of course in circuits where a small value of /?' is tolerable, a more reasonable value of inductance may be used. In low time constant applications, a small inexpensive air-cored inductor may be used.

Figure 1.73(a) shows the *RL* low-pass circuit. At very low frequencies the reactance of the inductor is small, so the output across the resistor /?' is almost equal to the input. As the frequency increases, the reactance of the inductor increases and so the signal is attenuated. At

very high frequencies the output is almost equal to zero. So the circuit in Figure 1.73(a) acts as a low-pass filter.The circuit of Figure 1.73(b) acts as a high-pass circuit because at low frequencies, since the reactance of the inductor is small, the output across the inductor is small and the output increases as the frequency increases because the reactance of the inductor increases as the frequency increases and at high frequencies the output is almost equal to the input.

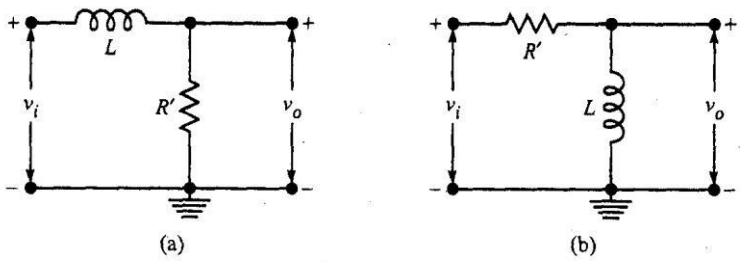


Figure 1.73 (a) *RL* low-pass circuit and (b) *RL* high-pass circuit.

RLC CIRCUITS

RLC Series Circuit

Consider a series *RLC* circuit shown in Figure 1.75.

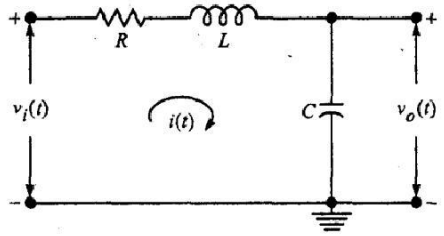


Figure 1.75 A series *RLC* circuit.

Writing the KVL around the loop, we obtain

$$v_i(t) = Ri(t) + L\frac{di(t)}{dt} + \frac{1}{C}\int i(t)\,dt$$

Taking the Laplace transform on both sides,

$$V_i(s) = I(s)\left[R + Ls + \frac{1}{Cs}\right] = \frac{I(s)}{Cs}[LCs^2 + RCs + 1]$$

$$V_o(s) = I(s)\frac{1}{Cs}$$

The transfer function of the circuit of Figure 1.75 is

$$\frac{V_o(s)}{V_i(s)} = \frac{1}{LC\left[s^2 + \frac{R}{L}s + \frac{1}{LC}\right]}$$

The roots of the characteristic equation s_1 and s_2 are the values of s satisfying the equation

$$s^2 + \frac{R}{L}s + \frac{1}{LC} = 0$$

$$\therefore \quad s_1, s_2 = \frac{-R}{2L} \pm \sqrt{\left(\frac{R}{2L}\right)^2 - \frac{1}{LC}}$$

If $(R/2L)^2 > 1/LC$, i.e. $R > 2\sqrt{L/C}$, both the roots are real and different. The circuit is overdamped and there are no oscillations in the output. If $(R/2L)^2 = 1/LC$, i.e. $R = 2\sqrt{L/C}$, both the roots are real and equal. The circuit is critically damped. If $(R/2L)^2 < 1/LC$, i.e. $R < 2\sqrt{L/C}$, the roots are complex conjugate of each other. The circuit is underdamped and there will be oscillations in the output. The output is a sinusoid whose amplitude decays with time.

The term $\sqrt{L/C}$ is known as the *characteristic impedance* of the circuit.

For a step input of amplitude V, $V_i(s) = \frac{V}{s}$

$$\therefore \quad V_o(s) = \left(\frac{V}{LC}\right)\left(\frac{1}{s\left[s^2 + \frac{R}{L}s + \frac{1}{LC}\right]}\right)$$

and

$$I(s) = \frac{V}{L\left[s^2 + \frac{R}{L}s + \frac{1}{LC}\right]}$$

The current response is:

Case (a): overdamped circuit, $R > 2\sqrt{L/C}$

$$i(t) = \frac{V}{2AL}\left[e^{-s_1 t} - e^{-s_2 t}\right], \quad \text{here } s_1 > s_2$$

where $A = \sqrt{\left(\frac{R}{2}\right)^2 - \frac{1}{LC}}$

Case (b): critically damped circuit, $R = 2\sqrt{L/C}$

$$i(t) = \frac{Vt}{L}e^{-Rt/2L}$$

Case (c): underdamped circuit, $R < 2\sqrt{L/C}$

$$i(t) = \frac{V}{BL}e^{-Rt/2L} \sin Bt \quad \text{where } B = \sqrt{\frac{1}{LC} - \left(\frac{R}{2L}\right)^2}$$

The response of $i(t)$ and the response of $v_0(t)$ for the above three cases are shown in Figures 1.76(a) and 1.76(b) respectively.

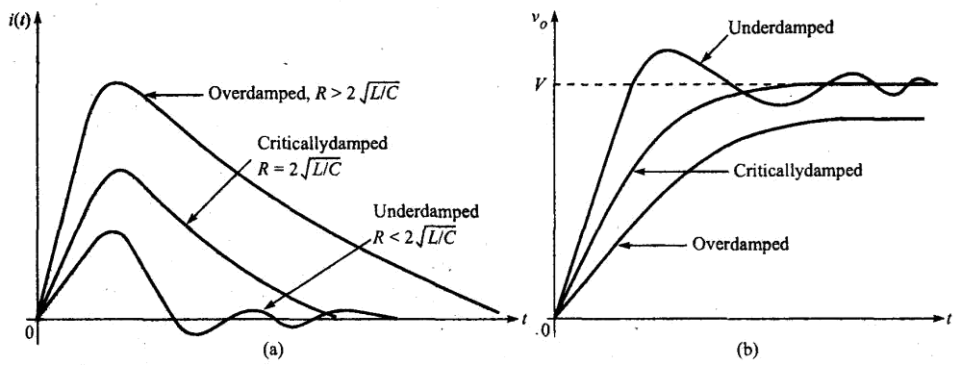


Figure 1.76 (a) Current response and (b) voltage response of series *RLC* circuit to a step voltage.

RLC Parallel Circuit

In the *RL* circuit shown in Figure 1.73(b), to include the effect of coil winding capacitance, output capacitance and stray capacitance to ground, a capacitor is added across the output. So, the *RLC* circuit shown in Figure 1.77(a) results. In terms of a current source, the equivalent circuit shown in Figure 1.77(b) results.

The transfer function of the network of Figure 1.77(a) is

$$\frac{V_o(s)}{V_i(s)} = \frac{1}{RC}\left(\frac{s}{s^2 + \frac{1}{RC}s + \frac{1}{LC}}\right)$$

The roots of the characteristic equation are

$$s_1, s_2 = -\frac{1}{2RC} \pm \sqrt{\left(\frac{1}{2RC}\right)^2 - \frac{1}{LC}}$$

These are also the characteristic roots of the network in Figure 1.77(b).

The circuit is overdamped if $R < \frac{1}{2}\sqrt{L/C}$, critically damped if $R = \frac{1}{2}\sqrt{L/C}$ and underdamped if $R > \frac{1}{2}\sqrt{L/C}$. The response to the voltage across the *RLC* parallel circuit is similar to that to the current through the *RLC* series circuit with the difference that the input to the *RLC* parallel circuit is a step current.

In the series *RLC* network, the current response to a step input voltage ultimately dies to zero because of the capacitor in series. In the parallel *RLC* circuit the voltage across the *RLC* network is zero because of the inductance.

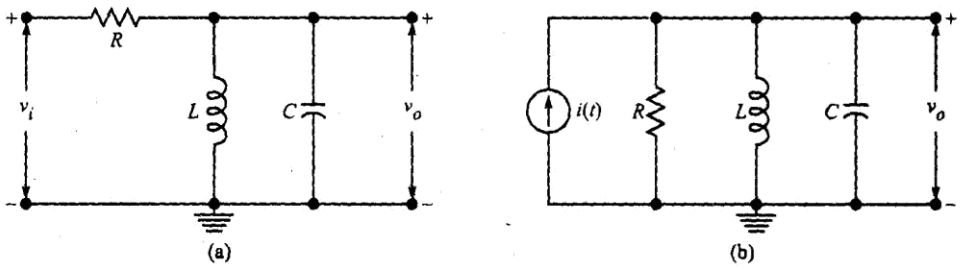


Figure 1.77 (a) v_i is applied through R to a parallel LC circuit and (b) parallel RLC circuit driven by a current source.

UNIT – II

NON LINEAR WAVESHAPING

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Diode clippers, Transistor clippers, clipping at two independent levels, Transfer characteristics of clippers, Emitter coupled clipper, Comparators, applications of voltage comparators, clamping operation, clamping circuits using diode with different inputs, Clamping circuit theorem, practical clamping circuits, effect of diode characteristics on clamping voltage, Transfer characteristics of clampers.

……

In the previous chapter we discussed about linear wave shaping. We saw how a change of wave shape was brought about when a non-sinusoidal signal is transmitted through a linear network like *RC* low pass and high pass circuit. In this chapter, we discuss some aspects of nonlinear wave shaping like clipping and clamping. The circuits for which the outputs are non-sinusoidal for sinusoidal inputs are called nonlinear wave shaping circuits, for example clipping circuits and clamping circuits.

Clipping means cutting and removing a part. A clipping circuit is a circuit which removes the undesired part of the waveform and transmits only the desired part of the signal which is above or below some particular reference level, i.e. it is used to select for transmission that part of an arbitrary waveform which lies above or below some particular reference. Clipping circuits are also called *voltage* (or current) *limiters, amplitude selectors* or *slicers.*

Nonlinear wave shaping circuits may be classified as clipping circuits and clamping circuits. Clipping circuits may be single level clippers or two level clippers.

Single level clippers may be series diode clippers with and without reference or shunt diode clippers with and without reference. Clipping circuits may use diodes or transistors.

Clamping circuits may be negative clampers (positive peak clampers) with and without reference or positive clampers (negative peak clampers) with and without reference.

CLIPPING CIRCUITS

In general, there are three basic configurations of clipping circuits.

1. A series combination of a diode, a resistor and a reference voltage.
2. A network consisting of many diodes, resistors and reference voltages.
3. Two emitter coupled transistors operating as a differential amplifier.

Diode Clippers

Figure 2.1(a) shows the v-i characteristic of a practical diode. Figures 2.1(b), (c), (d), and (e) show the *v-i* characteristics of an idealized diode approximated by a curve which is piece-wise linear and continuous. The break point occurs at V_r, where V_r = 0.2 V for Ge and V_r = 0.6 V for Si. Usually V_r is very small compared to the reference voltage V_R and can be neglected.

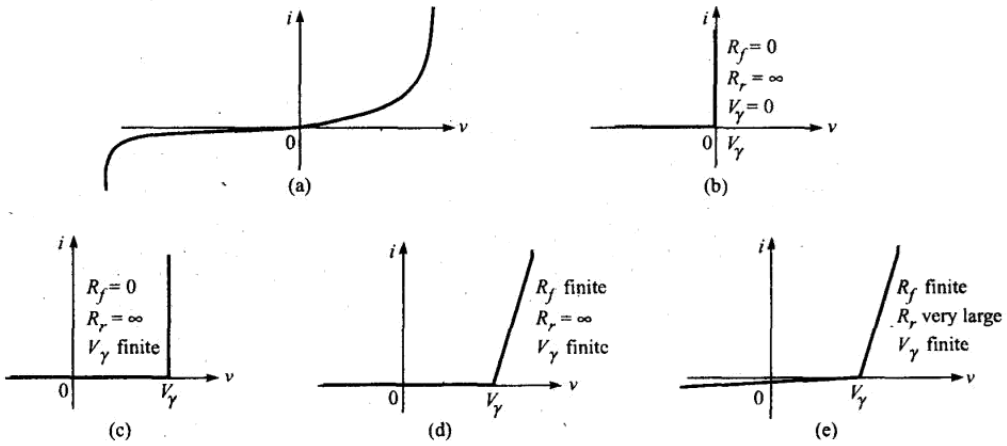


Figure 2.1 *v–i* characteristics of a diode.

Shunt Clippers

Clipping above reference level

Using the ideal diode characteristic of Figure 2.2(a), the clipping circuit shown in Figure 2.2(b), has the transmission characteristic shown in Figure 2.2(c). The transmission characteristic which is a plot of the output voltage v_0 as a function of the input voltage v, also exhibits piece-wise linear discontinuity. The break point occurs at the reference voltage V_R. To the left of the break point i.e. for $v_t < V_R$ the diode is reverse biased (OFF) and the equivalent circuit shown in Figure 2.2(d) results. In this region the signal v, may be transmitted directly to the output, since there is no load across the output to cause a drop across the series resistor /?. To the right of the break point i.e. for $v_($ > V_R the diode is forward biased (ON) and the equivalent circuit shown in Figure 2,2(e) results and increments in the inputs are totally attenuated and the output is fixed at V_R. Figure 2.2(c) shows a sinusoidal input signal of amplitude large enough so that the signal makes excursions past the break point. The corresponding output exhibits a suppression of the positive peak of the signal. The output will appear as if the positive peak had been *clipped off* or *sliced off*

Clipping below reference level

If this clipping circuit of Figure 2.2(b), is modified by reversing the diode as shown in Figure 2.3(a), the corresponding piece-wise linear transfer characteristic and the output for a sinusoidal input will be as shown in Figure 2.3(b). In this circuit, the portion of the waveform more positive than V_R is transmitted without any attenuation but the portion of the waveform less positive than V_R is totally suppressed. For Vj < V_R, the diode conducts and acts as a short circuit and the equivalent circuit shown in Figure 2.3(c) results and the output is fixed at V_R. For v, > V_R, the diode is reverse biased and acts as an open circuit and the equivalent circuit shown in Figure 2.3(d) results and the output is the same as the input.

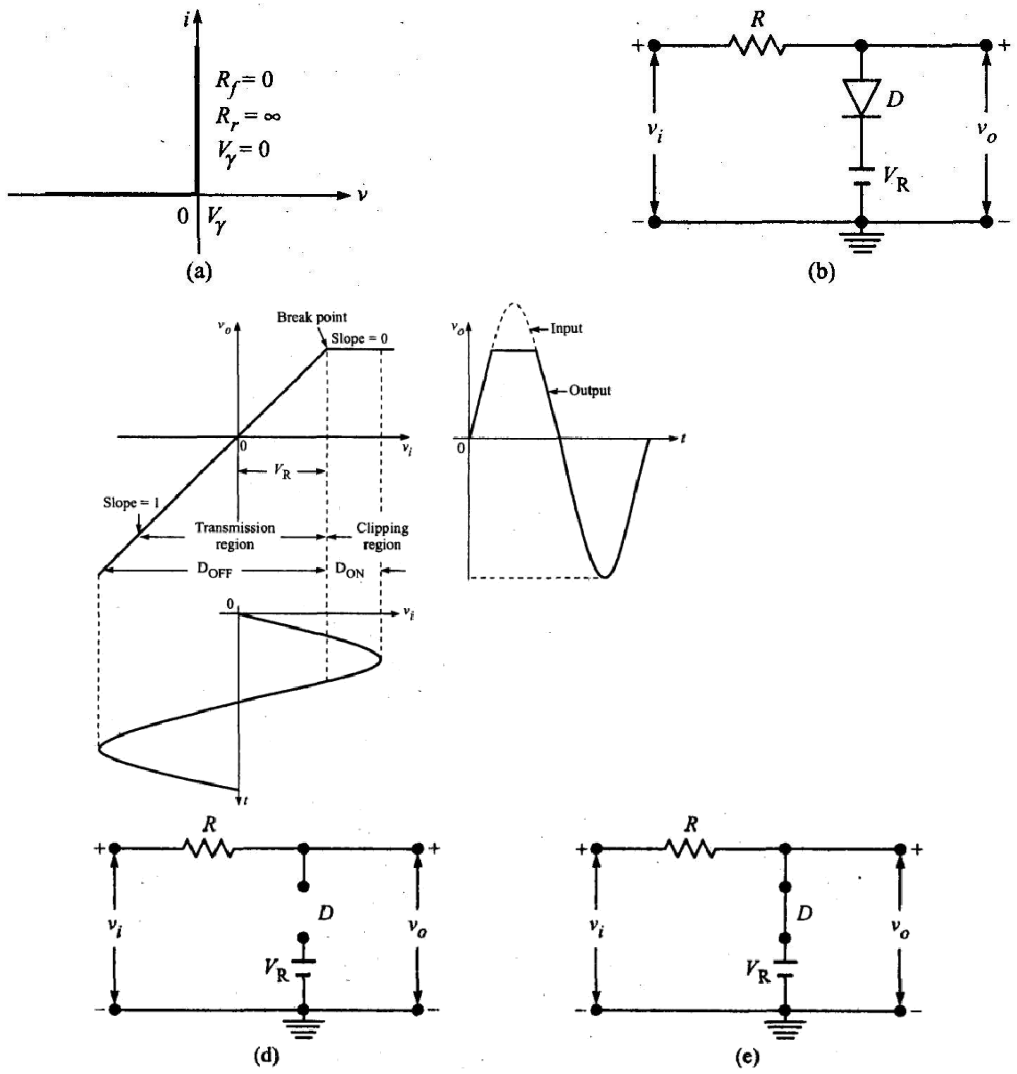


Figure 2.2 (a) *v-i* characteristic of an ideal diode, (b) diode clipping circuit, which removes that part of the waveform that is more positive than V_R, (c) the piece-wise linear transmission characteristic of the circuit, a sinusoidal input and the clipped output, (d) equivalent circuit for v(< V_R, and (e) equivalent circuit for v, > V_R.

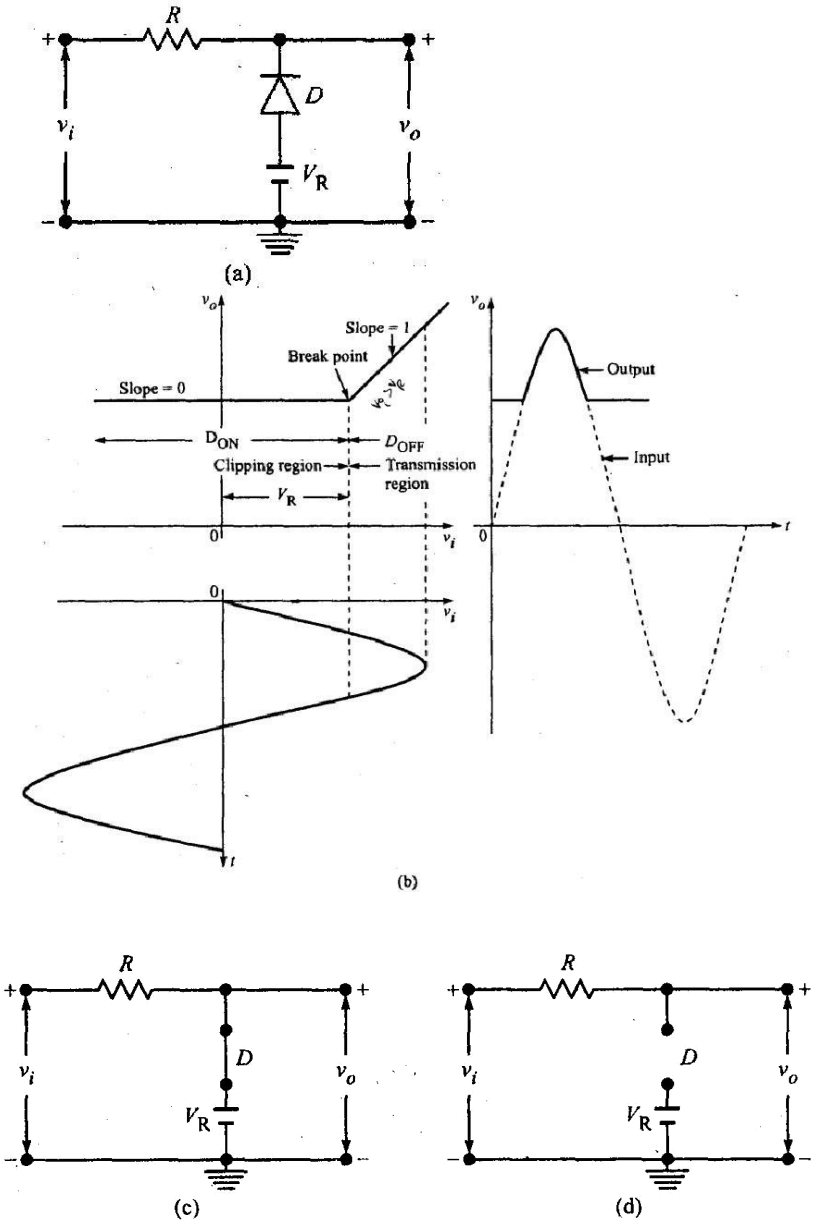


Figure 2.3 (a) A diode clipping circuit, which transmits that part of the sine wave that is more positive than VR, (b) the piece-wise linear transmission characteristic, a sinusoidal input and the clipped output, (c) equivalent circuit for $v_(< V_R$, and (d) equivalent circuit for v,- > VR.

In Figures 2.1(b) and 2.2(a), we assumed that R_r = °° and R_f = 0. If this condition does not apply, the transmission characteristic must be modified. The portions of those curves which are indicated as having unity slope must instead be considered as having a slope of $R_r l(R_r + R)$, and those, having zero slope as having a slope of /?/(/?/ + /?). In the transmission region of a diode clipping circuit, it is required that $R_r » R$, i.e. $R_r = kR$, where k is a large number, and in the attenuation region, it is required that $R » Rf$. From

these equations we can deduce that $R = J\ R_r x R^{\wedge}$, i.e. the external resistance R is to be selected as the geometric mean of Rf and /?,. The ratio $R_r IRf$ serves as a figure of merit for the diodes used in these applications. A zener diode may also be used in combination with a *p-n* junction diode to obtain single-ended clipping, i.e. one-level clipping.

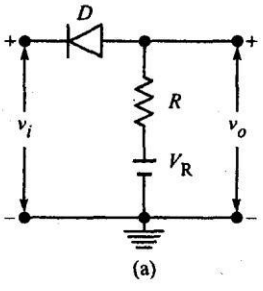
Series Clippers

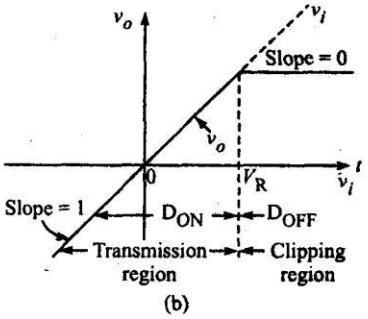
Clipping above the reference voltage V_n

Figure 2.4(a) shows a series clipper circuit using a p-n junction diode. V_R is the reference voltage source. The diode is assumed to be ideal (/?/ = 0, R_r = °°, V_y= 0) so that it acts as a short circuit when it is ON and as a open circuit when it is OFF. Since the diode is in the series path connecting the input and the output it is called a series clipper. The v_0 versus v, characteristic called the *transfer characteristic* is shown in Figure 2.4(b). The output for a sinusoidal input is shown in Figure 2.4(c).

The circuit works as follows:

For v, < V_R, the diode Dj is forward biased because its anode is at a higher potential than its cathode. It conducts and acts as a short circuit and the equivalent circuit shown in Figure 2.4(d) results. The difference voltage between the input v,- and the reference voltage V_R i.e. (V_R – v_i) is dropped across . Therefore $v_0 = v_i$ and the slope of the transfer characteristic for $v_i < V_R$ is 1. Since the input signal is transmitted to the output without any change, this region is called the transmission region.





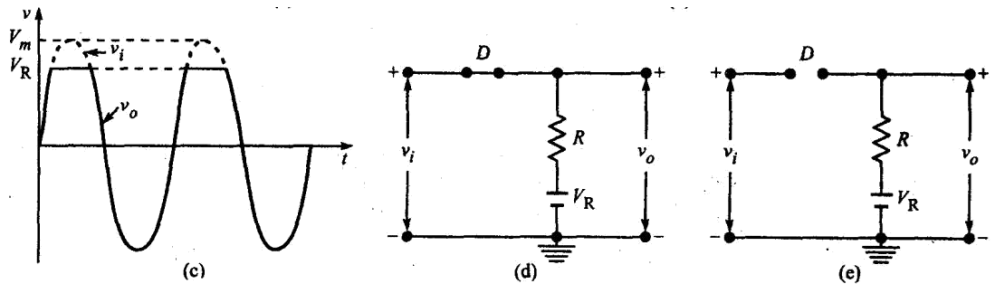
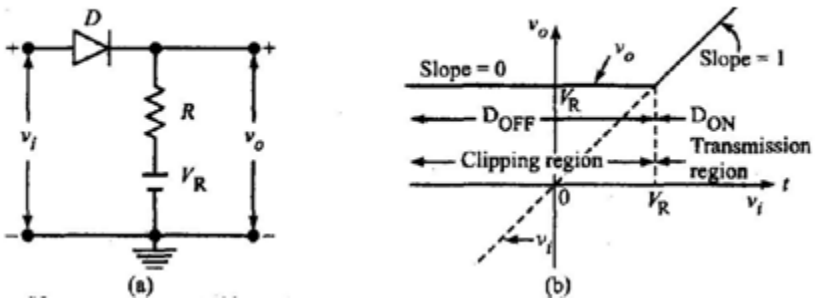


Figure 2.4 (a) Diode series clipper circuit diagram, (b) transfer characteristic, (c) output waveform for a sinusoidal input, (d) equivalent circuit for $v_; < V_R$, and (e) equivalent circuit for $v_(> V_R$.

For v, > V_R, the diode is reverse biased because its cathode is at a higher potential than its anode, it does not conduct and acts as an open circuit and the equivalent circuit shown in Figure 2.4(e) results. No current flows through *R* and so no voltage drop across it. So the output voltage v_0 = VR and the slope of the transfer characteristic is zero. Since the input signal above V_R is clipped OFF for v, > V_R, this region is called the *clipping region.* The equations $V_0=V_i$ for $V_i < V_R$ and $V_0= V_R$ for $V_i > V_R$ are called the transfer characteristic equations.

Clipping below the reference voltage V_B

Figure 2.5(a) shows a series clipper circuit using a p-n junction diode and a reference voltage source V_R. The diode is assumed to be ideal *(Rf* = 0, R_r = °°, V_y = 0) so that it acts as a short circuit when it is ON and as a open circuit when it is OFF. Since the diode is in the series path connecting the input and the output it is called a series clipper. The transfer characteristic is shown in Figure 2.5(b). The output for a sinusoidal input is shown in Figure 2.5(c).



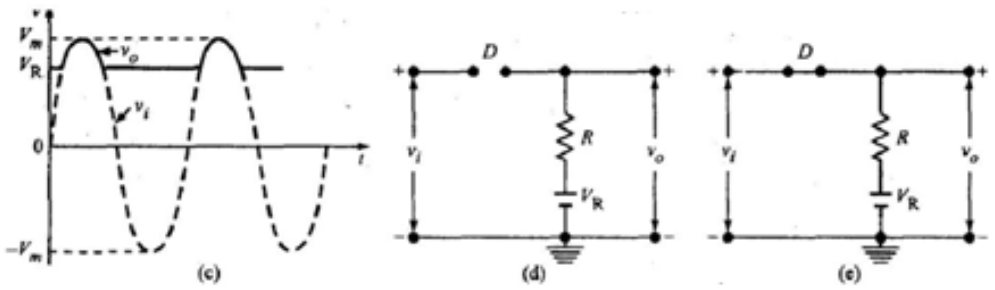


Figure 2.5 (a) Diode series clipper circuit diagram, (b). transfer characteristics, (c) output for a sinusoidal input, (d) equivalent circuit for v_i- < V_R, and (e) equivalent circuit for v_i- > VR.

The circuit works as follows:

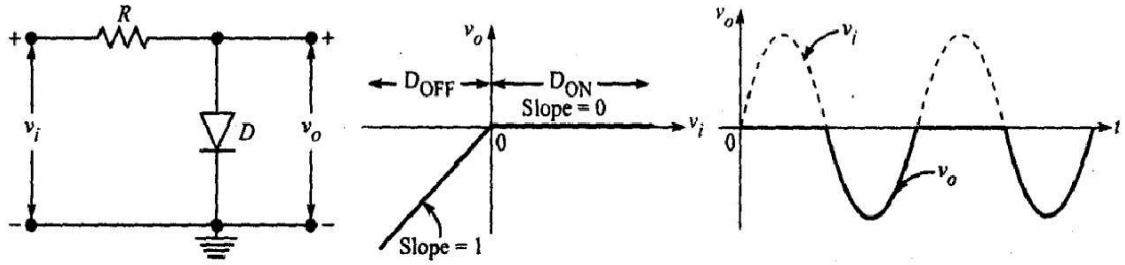
For v_i < V_R, D is reversed biased because its anode is at a lower potential than its cathode. The diode does not conduct and acts as an open circuit and the equivalent circuit shown in Figure 2.5(d) results. No current flows through *R* and hence no voltage drop across *R* and hence v_o = VR- So the slope of the transfer characteristic is zero for v, < V_R. Since the input is clipped off for v, < V_R, this region is called the clipping region.

For v, > VR, the diode is forward biased because its anode is at a higher potential than its cathode. The diode conducts and acts as a short circuit and the equivalent circuit shown in Figure 2.5(e) results. Current flows through /? and the difference voltage between the input and the output voltages v, - VR drops across /? and the output v_0 = v_i. The slope of the transfer characteristic for v, > VR is unity. Since the input is transmitted to the output for v; > V_R, this region is called the transmission region. The equations are called the transfer characteristic equations.

$v_o = V_R$ for $v_i < V_R$
$v_o = v_i$ for $v_i > V_R$

Some single-ended diode clipping circuits, their transfer characteristics and the output waveforms for sinusoidal inputs are shown below (Figure 2.6).

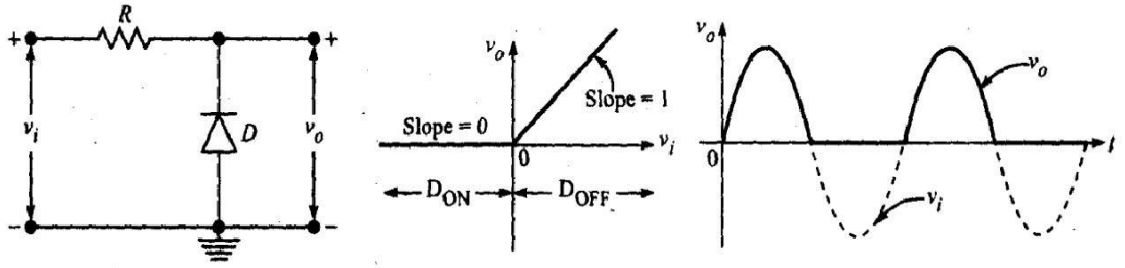
Some single-ended clipping circuits



For $v_i < 0$, D is OFF, $\therefore v_o = v_i$

For $v_i > 0$, D is ON, $\therefore v_o = 0$

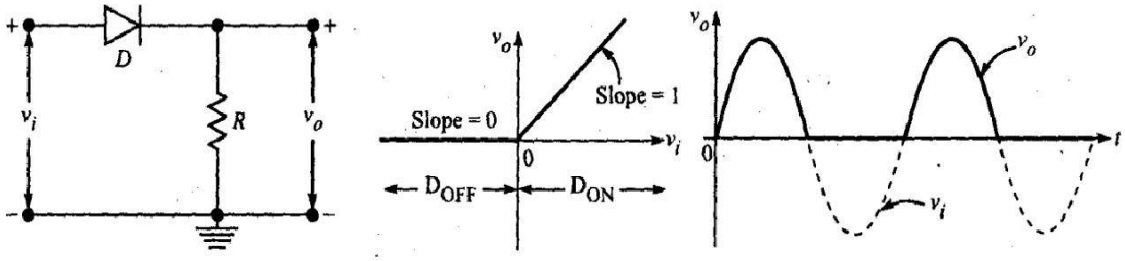
(a) Shunt clipper, positive peak clipping without reference



For $v_i < 0$, D is ON, $\therefore v_o = 0$

For $v_i > 0$, D is OFF, $\therefore v_o = v_i$

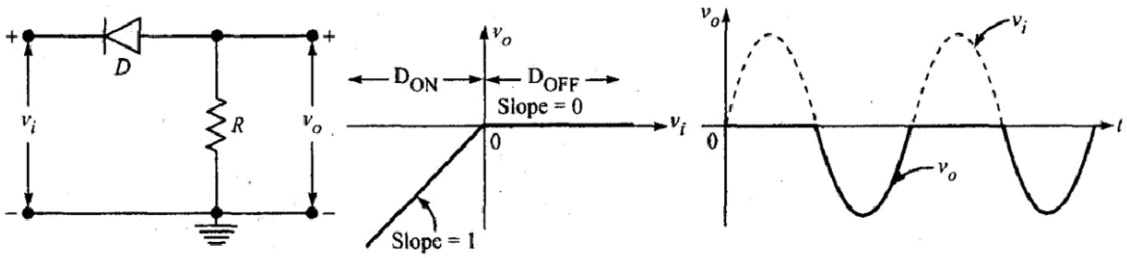
(b) Shunt clipper, negative peak clipping without reference



For $v_i < 0$, D is OFF, $\therefore v_o = 0$

For $v_i > 0$, D is ON, $\therefore v_o = v_i$

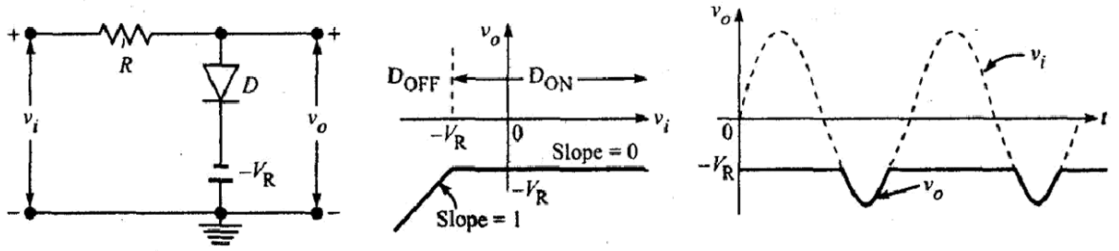
(c) Series clipper, negative peak clipping without reference



For $v_i < 0$, D is ON $\therefore v_o = v_i$

For $v_i > 0$, D is OFF $\therefore v_o = 0$

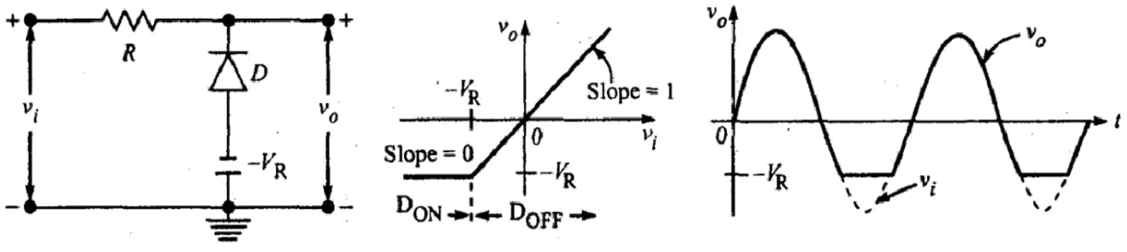
(d) Series clipper, positive peak clipping without reference



For $v_i < -V_R$, D is OFF $\therefore v_o = v_i$

For $v_i > -V_R$, D is ON $\therefore v_o = -v_i$

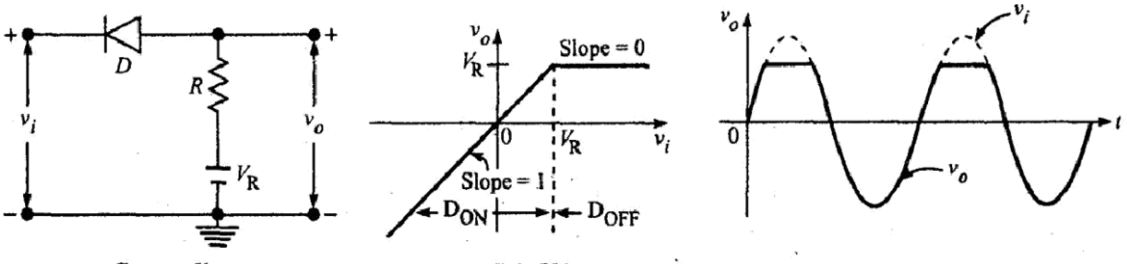
(e) Shunt clipper, negative base clipping above reference level



For $v_i < -V_R$, D is ON $\therefore v_o = -V_R$

For $v_i > -V_R$, D is OFF $\therefore v_o = v_i$

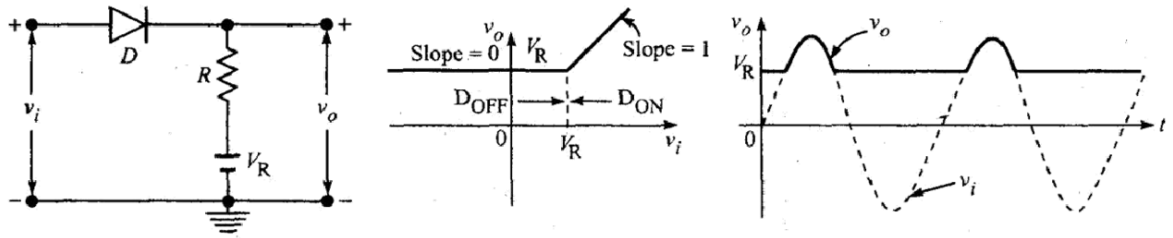
(f) Shunt clipper, negative base clipping below reference level



For $v_i < V_R$, D is ON $\therefore v_o = v_i$

For $v_i > V_R$, D is OFF $\therefore v_o = V_R$

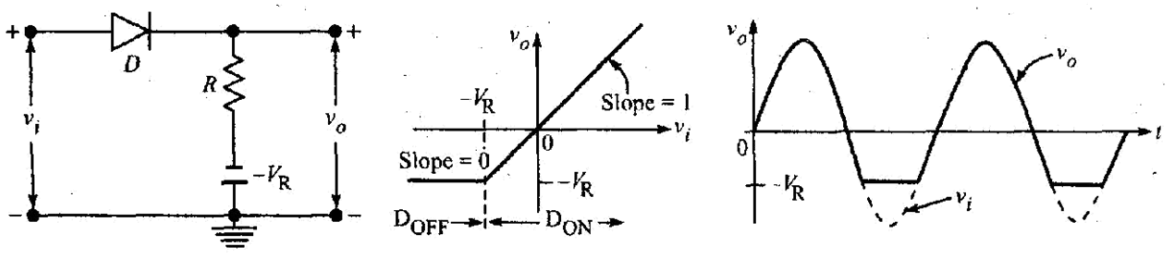
(g) Series clipper, positive base clipping above reference level



For $v_i < V_R$, D is OFF, $\therefore v_o = V_R$

For $v_i > V_R$, D is ON, $\therefore v_o = v_i$

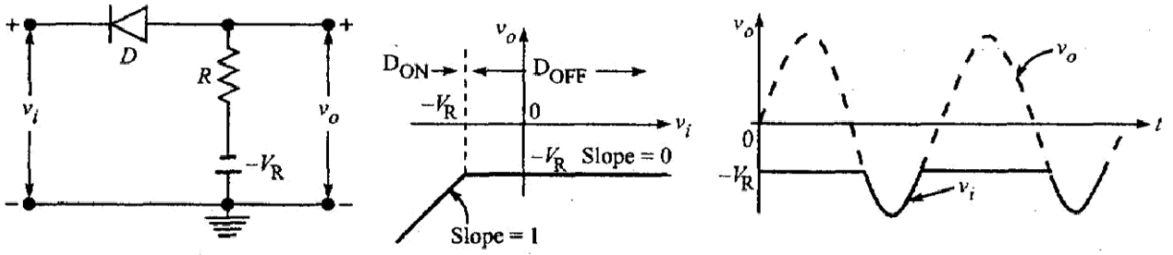
(h) Series clipper, positive base clipping before reference level



For $v_i < -V_R$, D is OFF, $\therefore v_o = -V_R$

For $v_i > -V_R$, D is ON, $\therefore v_o = v_i$

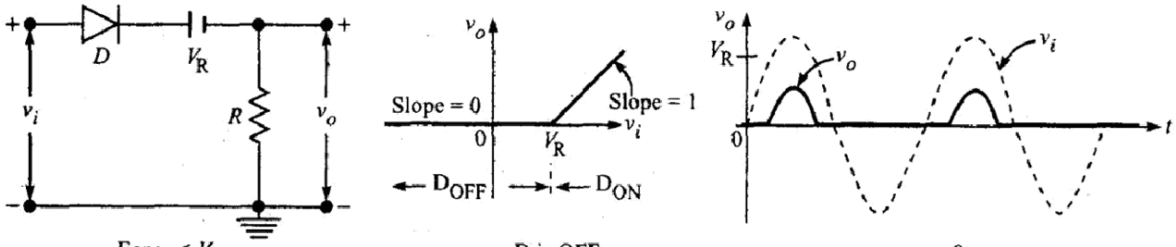
(i) Series clipper, negative base clipping above reference level



For $v_i < -V_R$, D is ON, $\therefore v_o = v_i$

For $v_i > -V_R$, D is OFF, $\therefore v_o = -V_R$

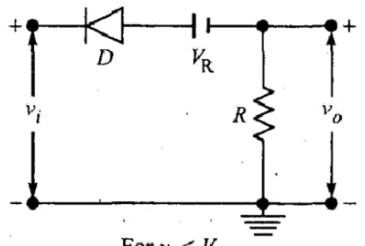
(j) Series clipper, negative base clipping above reference level



For $v_i < V_R$, D is OFF, $\therefore v_o = 0$

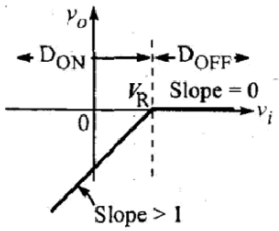
For $v_i > V_R$, D is ON, $\therefore v_o = v_i - V_R$

(k) Series clipper (Biased)



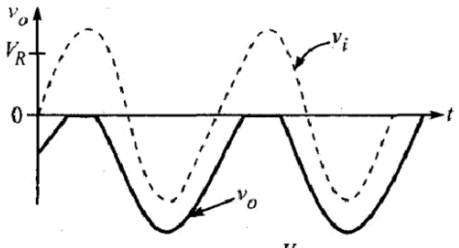
For $v_i < V_R$, $\therefore v_o = v_i - V_R$

For $v_i > V_R$, $\therefore v_o = 0$

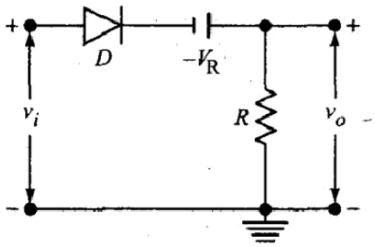


D is ON

D is OFF

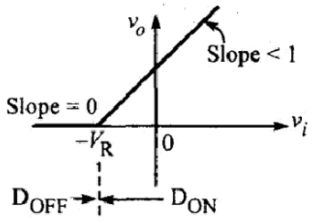


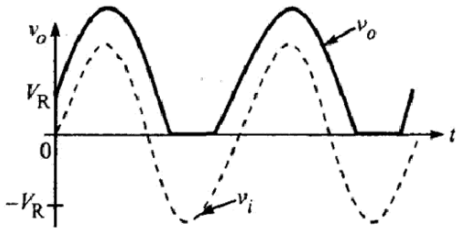
(l) Series clipper (Biased)



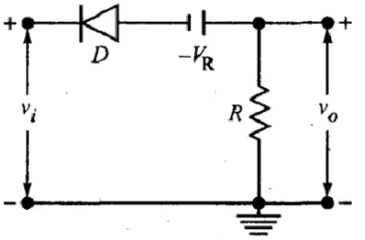
For $v_i < -V_R$, D is OFF $\therefore v_o = 0$

For $v_i > -V_R$, D is ON $\therefore v_o = v_i + V_R$



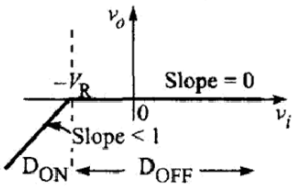


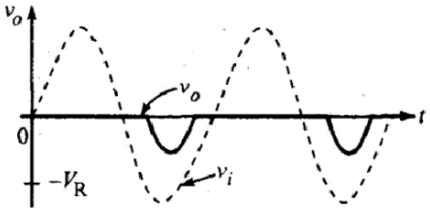
(m) Series clipper (Biased)



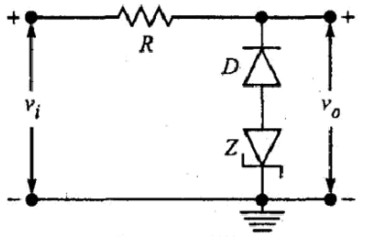
For $v_i < -V_R$, D is ON $\therefore v_o = v_i + V_R$

For $v_i > -V_R$, D is OFF $\therefore v_o = 0$



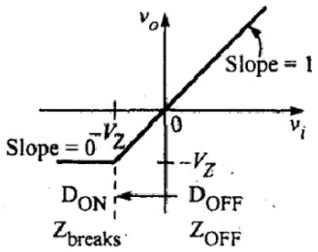


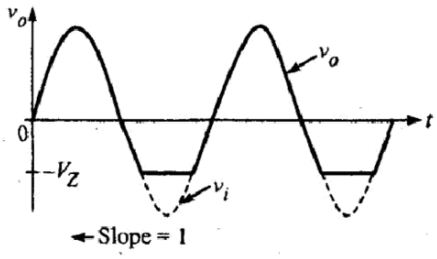
(n) Series clipper (Biased)



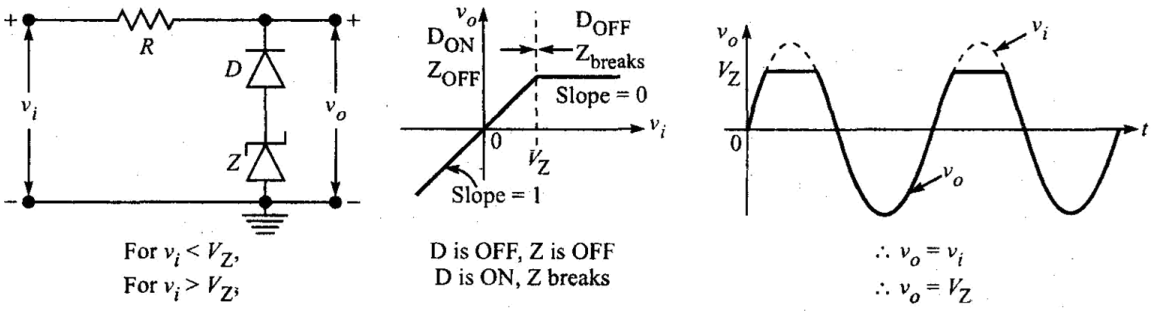
For $v_i < -V_Z$, D is ON, Z breaks $\therefore v_o = -V_Z$

For $v_i > -V_Z$, D is OFF, Z is OFF $\therefore v_o = v_i$





(o) Shunt clipper using zener diode, negative clipping



(p) Shunt clipper using zener diode, positive clipping

Figure 2.6 Examples of single-ended clipping circuits.

In the clipping circuits, the diode may appear as a series element or as a shunt element. The use of the diode as a series element has the disadvantage that when the diode is OFF and it is intended that there be no transmission, fast signals or high frequency waveforms may be transmitted to the output through the diode capacitance. The use of the diode as a shunt element has the disadvantage that when the diode is open and it is intended that there be transmission, the diode capacitance together with all other capacitances in shunt with the output terminals will round off the sharp edges of the input waveforms and attenuate, the high frequency signals.

Clipping at Two Independent Levels

A parallel, a series, or a series-parallel arrangement may be used in double-ended limiting at two independent levels. A parallel arrangement is shown in Figure 2.7. Figure 2.8 shows the transfer characteristic and the output for a sinusoidal input. The input-output characteristic has two breakpoints, one at v_0 = v, = V_{R1} and the second at v_0 = v, = -V_{R2} and has the following characteristics.

Input v_i	*Output* v_o	*Diode status*
$v_i > V_{R1}$	$v_o = V_{R1}$	D_1 ON, D_2 OFF
$-V_{R2} < v_i < V_{R1}$	$v_o = v_i$	D_1 OFF, D_2 OFF
$v_i < -V_{R2}$	$v_o = -V_{R2}$	D_1 OFF, D_2 ON

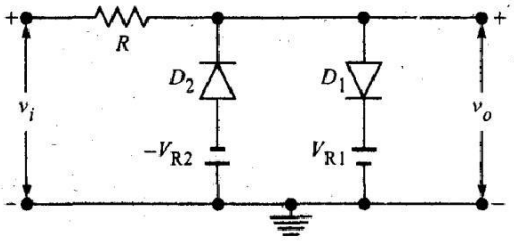


Figure 2.7 A diode clipper which limits at two independent levels.

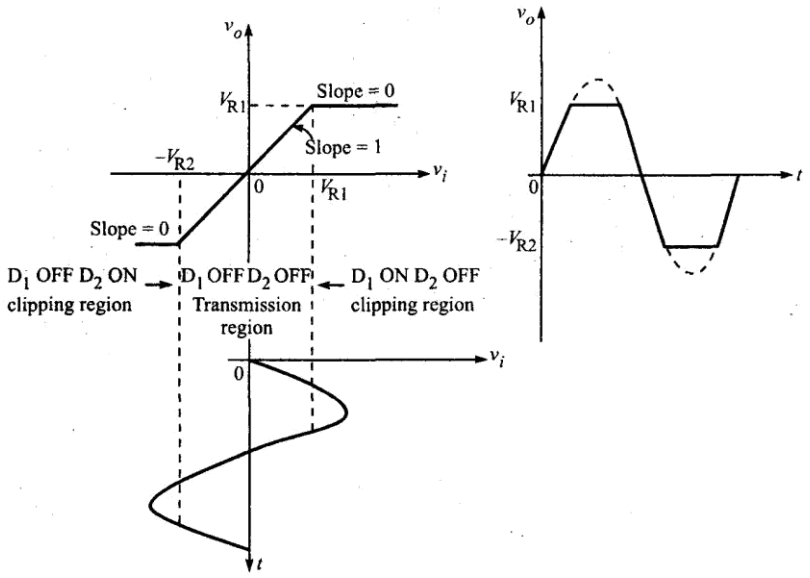


Figure 2.8 The piece-wise linear transfer curve, the input sinusoidal waveform and the corresponding output for the clipper of Figure 2.7.

The two level diode clipper shown in Figure 2.8 works as follows. For v, > V_{R1}, DI is ON and D_2 is OFF and the equivalent circuit shown in Figure 2.9(a) results. So the output v_0 = V_{R1} and the slope of the transfer characteristic is zero.

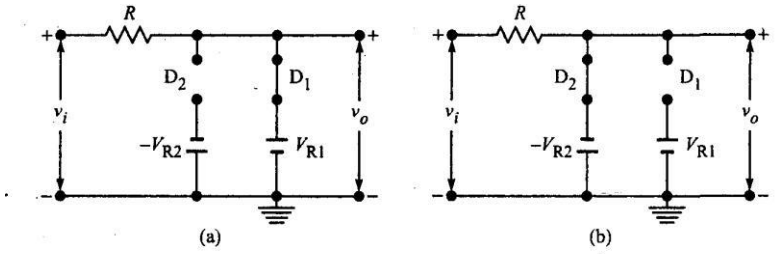


Figure 2.9 (a) Equivalent circuit for $v_i > V_{R1}$ and (b) equivalent circuit for $v_i < -V_{R2}$.

For v, < - V_{R2}, DI is OFF and D_2 is ON and the equivalent circuit shown in Figure 2.9(b) results. So the output v_0 = - V_{R2} and the slope of the transfer characteristic is zero. For-V_{R2} < v, < VRI, D! is OFF and D_2 is OFF and the equivalent circuit shown in Figure 2.10 results. So the output v_0 = v/ and the slope of the transfer characteristic is one.

The circuit of Figure 2.7 is called a slicer because the output contains a slice of the input between two reference levels $V_{R!}$ and V_{R2}. Looking at the input and output waveforms, we observe that this circuit may be used to convert a sine wave into a square wave, if VDI = Vm. and if the amplitude of the input signal is very large compared with the difference in the

reference levels, the output will be a symmetrical square wave. Two zener diodes in series opposing may also be used to form a double-ended clipper.

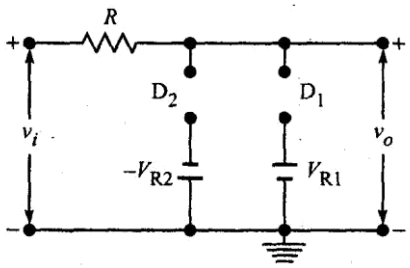
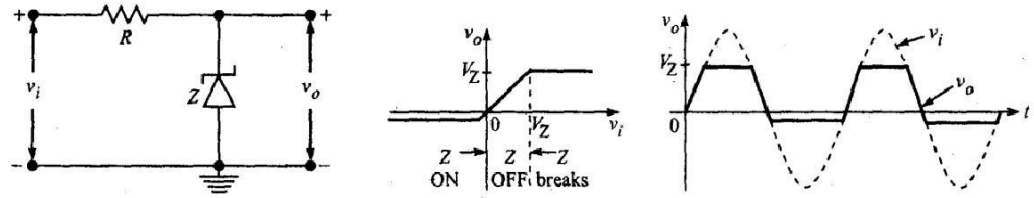


Figure 2.10 Equivalent circuit for $-V_{R2} < v_i < V_{R1}$.

If the diodes have identical characteristics, then, a symmetrical limiter is obtained. Some double-ended clippers, their transfer characteristics and the outputs for sine wave inputs are shown in Figure 2.11.

Some double-ended clipping circuits

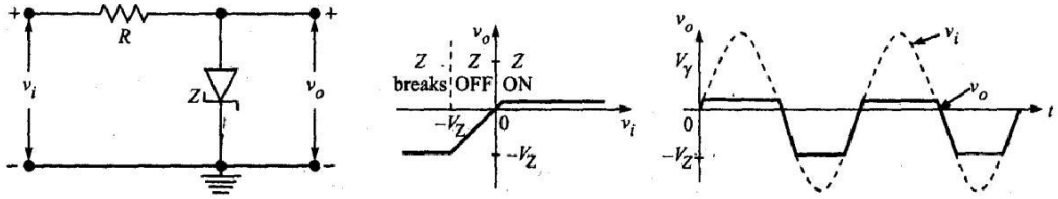


For $v_i < -V_\gamma$, Z is ON $\therefore v_o = -V_\gamma$

For $-V_\gamma < v_i < V_Z$, Z is OFF $\therefore v_o = v_i$

For $v_i > V_Z$, Z breaks $\therefore v_o = V_Z$

(a) Two level clipping using a zener diode

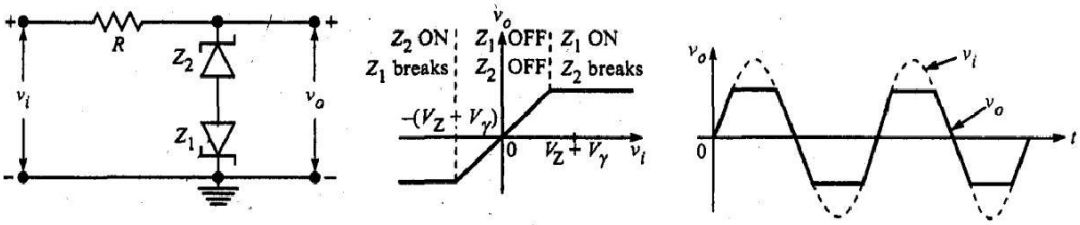


For $v_i < -V_Z$, Z breaks $\therefore v_o = -V_Z$

For $-V_Z < v_i < V_\gamma$, Z is OFF $\therefore v_o = v_i$

For $v_i > V_\gamma$, Z is ON $\therefore v_o = V_\gamma$

(b) Two level clipping using one zener diode

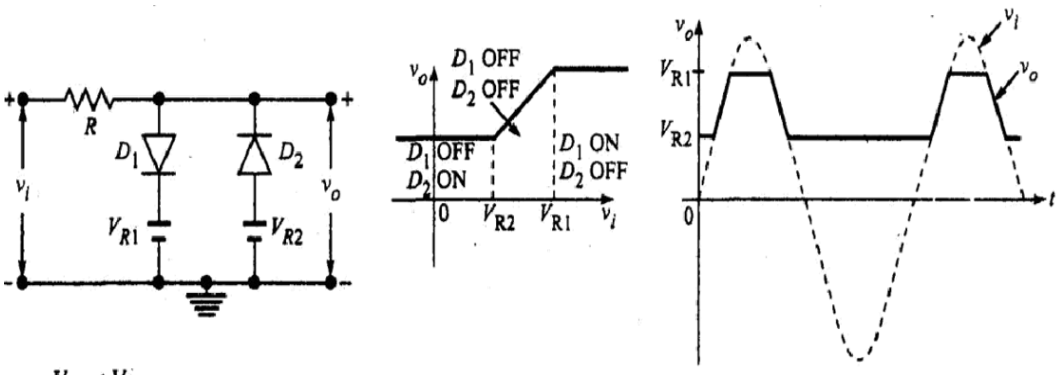


For $v_i < -(V_Z + V_\gamma)$, Z_1 breaks, Z_2 is on $\therefore v_o = -(V_Z + V_\gamma)$

For $-(V_Z + V_\gamma) < v_i < (V_Z + V_\gamma)$, Z_1 is OFF, Z_2 is OFF $\therefore v_o = v_i$

For $v_i > (V_Z + V_\gamma)$, Z_1 is ON, Z_2 breaks $\therefore v_o = V_Z + V_\gamma$

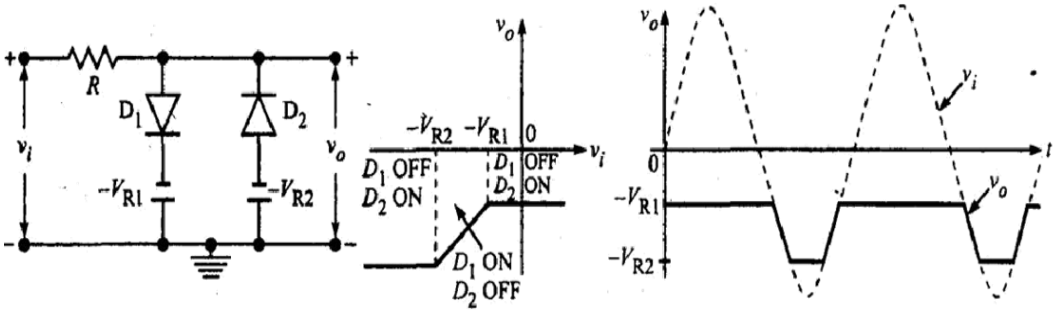
(c) Two level clipping using two zener diodes



$V_{R2} < V_{R1}$

For $v_i < V_{R2}$,	D_1 is OFF, D_2 is ON	$\therefore v_o = V_{R2}$
For $V_{R2} < v_i < V_{R1}$,	D_1 is OFF, D_2 is OFF	$\therefore v_o = v_i$
For $v_i > V_{R1}$,	D_1 is ON, D_2 is OFF	$\therefore v_o = V_{R1}$

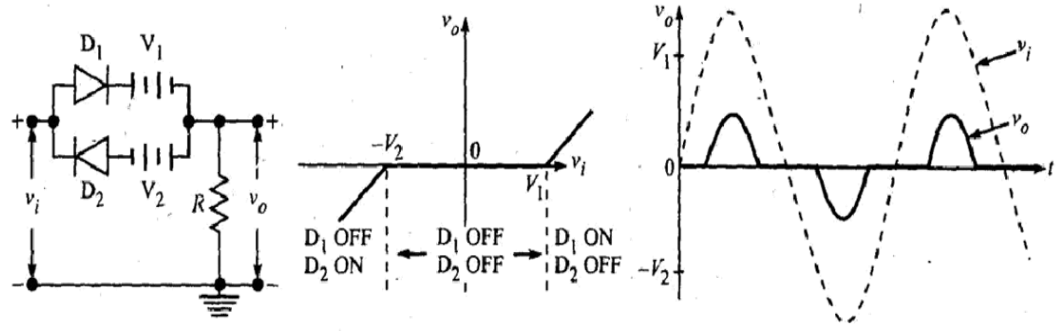
(d) Two level clipping using two diodes and two positive reference voltage sources.



$-V_{R2} < -V_{R1}$

For $v_i < -V_{R2}$,	D_1 is OFF, D_2 is ON	$\therefore v_o = -V_{R2}$
For $-V_{R2} < v_i < -V_{R1}$,	D_1 is OFF, D_2 is OFF	$\therefore v_o = v_i$
For $v_i > -V_{R1}$	D_1 is ON, D_2 is OFF	$\therefore v_o = -V_{R1}$

(e) Two level clipping using two diodes and two negative reference voltage sources.



For $v_i < -V_2$,	D_1 is OFF, D_2 is ON	$\therefore v_o = v_i + V_2$
For $-V_2 < v_i < V_1$,	D_1 is OFF, D_2 is OFF	$\therefore v_o = 0$
For $v_i > V_1$,	D_1 is ON, D_2 is OFF	$\therefore v_o = v_i - V_1$

(f) Double ended series biased clipper

Figure 2.11 Examples of double-ended clippers.

Transistor Clippers

A nonlinear device is required for clipping purposes. A diode exhibits a nonlinearity, which occurs when it goes from OFF to ON. On the other hand, the transistor has two pronounced nonlinearities, which may be used for clipping purposes. One occurs when the transistor crosses from the cut-in region into the active region and the second occurs when the transistor crosses from the active region into the saturation region. Therefore, if the peak-to-peak value of the input waveform is such that it can carry the transistor across the boundary between the cut-in and active regions, or across the boundary between the active and saturation regions, a portion of the input waveform will be clipped. Normally, it is required that the portion of the input waveform, which keeps the transistor in the active region shall appear at the output without distortion. In that case, it is required that the input current rather than the input voltage be the waveform of the signal of interest. The reason for this requirement is that over a large signal excursion in the active region, the transistor output current responds nominally linearly to the input current but is related in a quite nonlinear manner to the input voltage. So, in transistor clippers a current drive needs to be used.

A transistor clipper is shown in Figure 2.19. The resistor R which represents either the signal source impedance or a resistor deliberately introduced must be large compared with the input resistance of the transistor in the active region. Under these circumstances, the input base current will very nearly have the waveform of the input voltage, because the base current is given by $i_B = (v_i - V_\gamma)/R$ where V_r is the base-to-emitter cut-in voltage. V_y » 0.1 V for Ge and V_y ~ 0.5 V for Si.

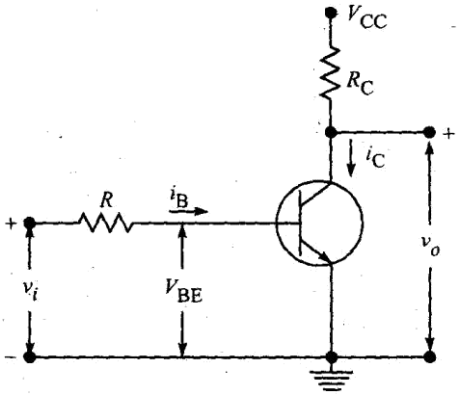


Figure 2.19 A transistor clipper.

If a ramp input signal v_i which starts at a voltage below cut-off and carries the transistor into saturation is applied, the base voltage, the base current, and the collector current waveforms of the transistor clipper will be as shown in Figure 2.20.

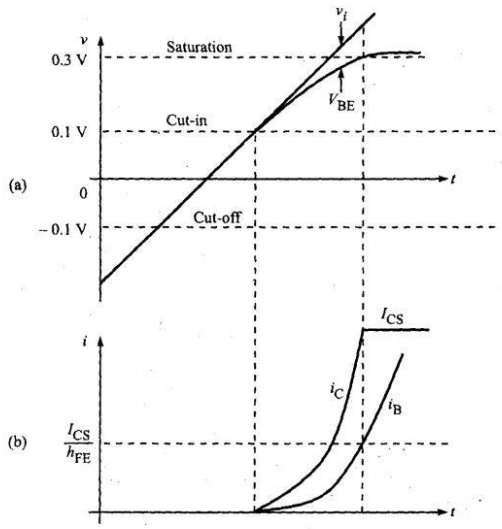


Figure 2.20 Waveforms of the transistor clipper of Figure 2.19: (a) voltage V_{BE} which results when a ramp input drives the transistor from cut-off into saturation, and (b) the base and collector currents.

The waveforms which result when a sinusoidal voltage v, carries the transistor from cut-off to saturation are shown in Figure 2.21. The base circuit is biased so that cut-in occurs when V_{BE} reaches the voltage *V*.

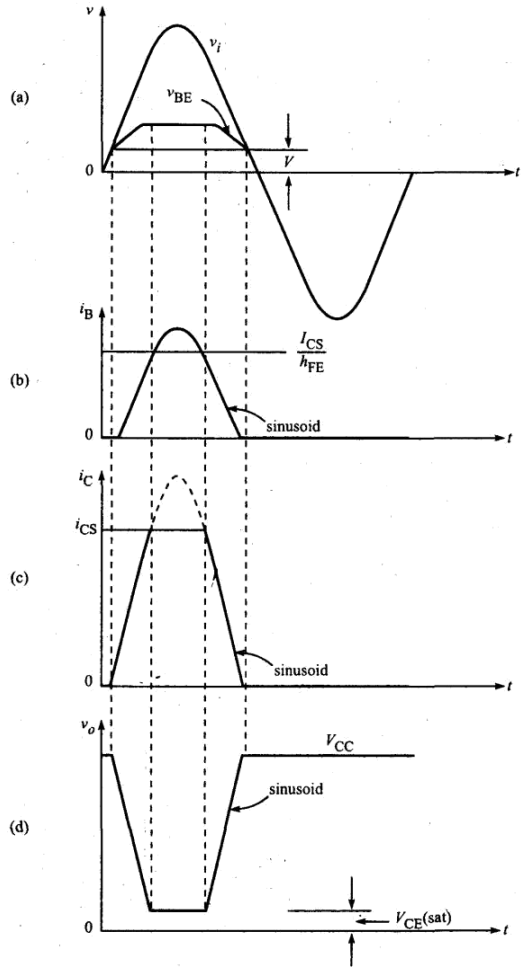


Figure 2.21 Waveforms for the transistor clipper of figure 2.19: (a) in put voltage and the base – to-emitter voltage (b) the base current (c) the collector current (d) the out put voltage

Emitter-Coupled Clipper

An emitter-coupled clipper is shown in Figure 2.22. It is a two-level clipper using transistors. The base of Q_2 is fixed at a voltage V_{BB2}, and the input is applied to B_1. If initially the input is negative, Q_1 is OFF and only Q_2 carries the current. Assume that V_{BB2} has been adjusted so that Q_2 operates in its active region. Let us assume that the current / in the emitter resistance is constant. This is valid if IV_BE_2I is small compared to $V_{BB2} + V_{EE}$ When v_t is below the cut-off point of Q_1, all the current 7 flows through Q_2. As v, increases, Q_1 will eventually come out of cut-off, both the transistors will be carrying currents but the current in Q_2 decreases while the current in Q_1 increases, the sum of the currents in the two transistors remaining constant and equal to 7. The input signal appears at the output, amplified but not inverted. As v_1 continues to increase, the common emitter will follow the base of Q_1. Since the base of Q_2 is fixed, a point will be reached when the rising emitter voltage cuts off Q_2. Thus, the input signal is amplified but twice limited, once by the cutoff of Q_1 and once by the onset of cut-off in Q_2. The total range Av_0, over which the output can follow the input is V_E and is constant and therefore adjustable through an adjustment of 7. The absolute voltage of the portion of the input waveform selected for transmission may be selected through an adjustment of a biasing voltage on which v, is superimposed or through an adjustment of V_{BB2}- The total range of input voltage Av, between the clipping limits is Av_0/A, where A is the gain of the amplifier stage. Figure 2.23 shows the transfer characteristic of an emitter-coupled clipper.

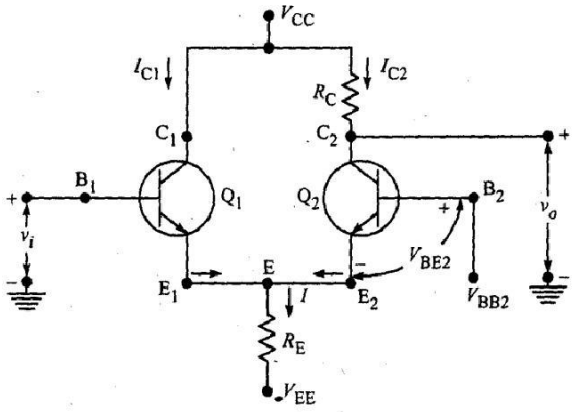


Figure 2.22 An emitter-coupled clipper.

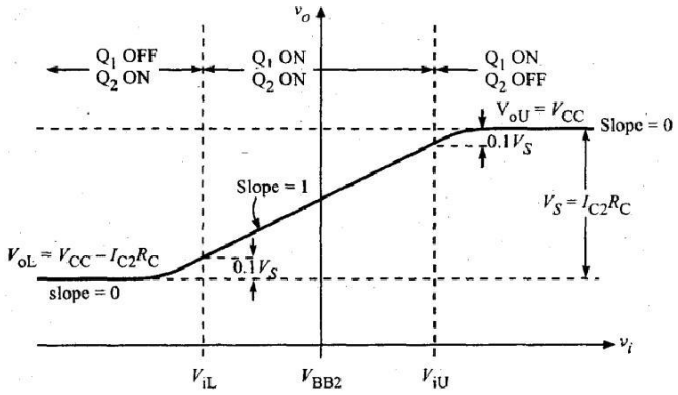


Figure 2.23 The transfer characteristic of the emitter-coupled clipper.

Comparators

A comparator circuit is one, which may be used to mark the instant when an arbitrary waveform attains some particular reference level. The nonlinear circuits, which can be used to perform the operation of clipping may also be used to perform the operation of comparison. In fact, the clipping circuits become elements of a comparator system and are Usually simply referred to as comparators. The distinction between comparator circuits and the clipping circuits is that, in a comparator there is 'no interest in reproducing any part of the signal waveform, whereas in a clipping circuit, part of the signal waveform is needed to be reproduced without any distortion.

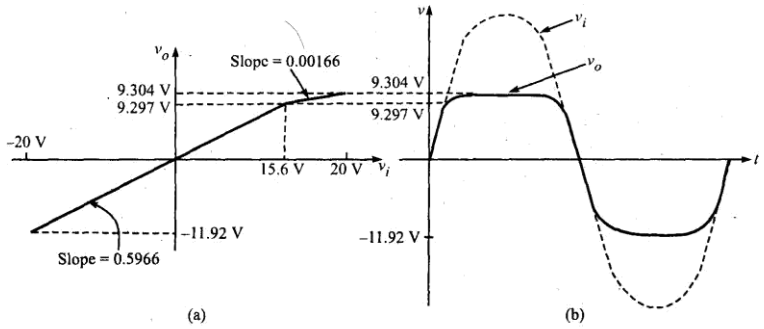


Figure 2.69 Example 2.19: (a) transfer characteristic and (b) output waveform in the presence of R_L.

Figure 2.70 shows the circuit diagram of a diode comparator. As long as the input voltage v, is less than the reference voltage V_R, the diode D is ON and the output is fixed at V_R. When v, > V_R, the diode is OFF and hence v_0 = v,. The break occurs at v, = V_R at time $t = t$\. So, this circuit can be used to mark the instant at which the input voltage reaches a particular reference level V_R.

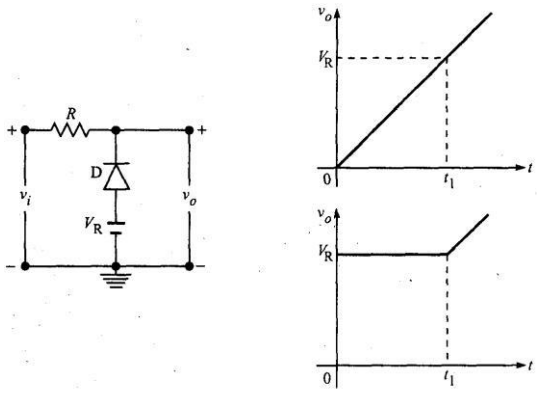


Figure 2.70 Diode comparator.

Comparators may be non-regenerative or regenerative. Clipping circuits fall into the category of non-regenerative comparators. In regenerative comparators, positive feedback is employed to obtain an infinite forward gain (unity loop gain). The Schmitt trigger and the blocking oscillator are examples of regenerative comparators. The Schmitt trigger comparator generates approximately a step input. The blocking oscillator comparator generates a pulse rather than a step output waveform. Most applications of comparators make use of the step or pulse natures of the input. Operational amplifiers and tunnel diodes may also be used as comparators.

Applications of voltage comparators

Voltage comparators may be used:

1. In accurate time measurements
2. In pulse time modulation
3. As timing markers generated from a sine wave.
4. In phase meters
5. In amplitude distribution analyzers
6. To obtain square wave from a sine wave
7. In analog-to-digital converters.

CLAMPING CIRCUITS

Clamping circuits are circuits, which are used to clamp or fix the extremity of a periodic waveform to some constant reference level V_R. Under steady-state conditions, these circuits restrain the extremity of the waveform from going beyond V_R. Clamping circuits may be one-way clamps or two-way clamps. When only one diode is used and a voltage change in only one direction is restrained, the circuits are called one-way clamps. When two diodes are used and the voltage change in both the directions is restrained, the circuits are called two-way clamps.

The Clamping Operation

When a signal is transmitted through a capacitive coupling network *(RC* high-pass circuit), it looses its dc component, and a clamping circuit may be used to introduce a dc component by fixing the positive or negative extremity of that waveform to some reference level. For this reason, the clamping circuit is often referred to as *dc restorer* or *dc reinserter.* In fact, it should be called a *dc inserter,* because the dc component introduced may be different from the dc component lost during transmission. The clamping circuit only changes the dc level of the input signal. It does not affect its shape

Classification of clamping circuits

Basically clamping circuits are of two types: (1) positive-voltage clamping circuits and (2) negative-voltage clamping circuits.

In positive clamping, the negative extremity of the waveform is fixed at the reference level and the entire waveform appears above the reference level, i.e. the output waveform is positively clamped with reference to the reference level. In negative clamping, the positive extremity of the waveform is fixed at the reference level and the entire waveform appears below the reference, i.e. the output waveform is negatively clamped with respect to the reference level. The capacitors are essential in clamping circuits. The difference between the clipping and clamping circuits is that while the clipper clipps off an unwanted portion of the input waveform, the clamper simply clamps the maximum positive or negative peak of the waveform to a desired level. There will be no distortion of waveform.

Negative Clamper

Figure 3.1 (a) shows the circuit diagram of a basic negative clamper. It is also termed a positive peak clamper since the circuit clamps the positive peak of a signal to zero level. Assume that the signal source has negligible output impedance and that the diode" is ideal, *Rf*= 0 n and V_y = 0 V in that, it exhibits an arbitrarily sharp break at 0 V, and that its input signal shown in Figure 2.71(b) is a sinusoid which begins at t = 0. Let the capacitor C be uncharged at t = 0.

During the first quarter cycle, the input signal rises from zero to the maximum value. The diode conducts during this time and since we have assumed an ideal diode, the voltage across it is zero. The capacitor *C* is charged through the series combination of the signal source and the diode and the voltage across C rises sinusoidally. At -the end of the first quarter cycle, the voltage across the capacitor, $v_C = V_m$.When, after the first quarter cycle, the peak has been passed and the input signal begins to fall, the voltage v_C across the capacitor is no longer able to follow the input, because there is no path for the capacitor to discharge. Hence, the voltage across the capacitor remains constant at $v_C = V_m$, and the charged capacitor acts as a voltage source of V volts and after the first quarter cycle, the output is given by v_0 = v, - V_m. During the succeeding cycles, the positive extremity of the signal will be *clamped* or *restored* to zero and the output

for $v_i = 0$, $v_o = -V_m$.
for $v_i = V_m$, $v_o = 0$,
for $v_i = -V_m$, $v_o = -2V_m$.

waveform shown in Figure 2.7 l(c) results. Therefore

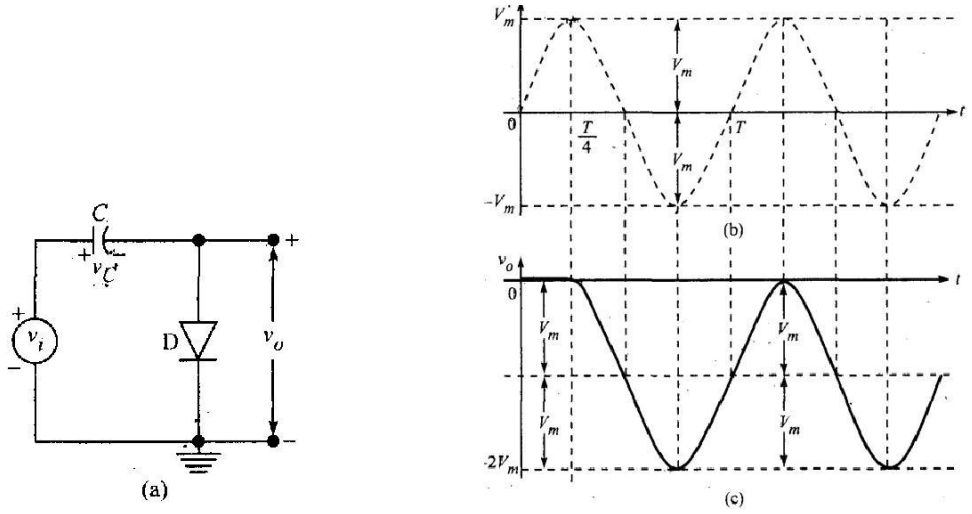


Figure 2.71 (a) A negative clamping circuit, (b) a sinusoidal input, and (c) a steady-state clamped output.

Suppose that after the steady-state condition has been reached, the amplitude of the input signal is increased, then the diode will again conduct for at most one quarter cycle and the dc voltage across the capacitor would rise to the new peak value, and the positive excursions of the signal would be again restored to zero.

Suppose the amplitude of the input signal is decreased after the steady-state condition has been reached. There is no path for the capacitor to discharge. To permit the voltage across the capacitor to decrease, it is necessary to shunt a resistor across *C*, or equivalently to shunt a

resistor across D. In the latter case, the capacitor will discharge through the series combination of the resistor *R* across the diode and the resistance of the source, and in a few cycles the positive extremity would be again clamped at zero as shown in Figure 2.72(b). A circuit with such a resistor *'R* is shown in Figure 2.72(a).

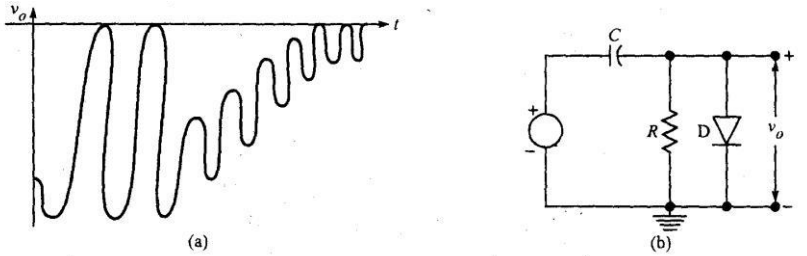


Figure 2.72 (a) Clamping circuit with a resistor *R* across the diode D and (b) output during transient period.

Positive Clamper

Figure 2.73(a) shows a positive clamper. This is also termed as negative peak clamper since this circuit clamps the negative peaks of a signal to zero level. The negative peak clamper, i.e. the positive clamper introduces a positive dc.

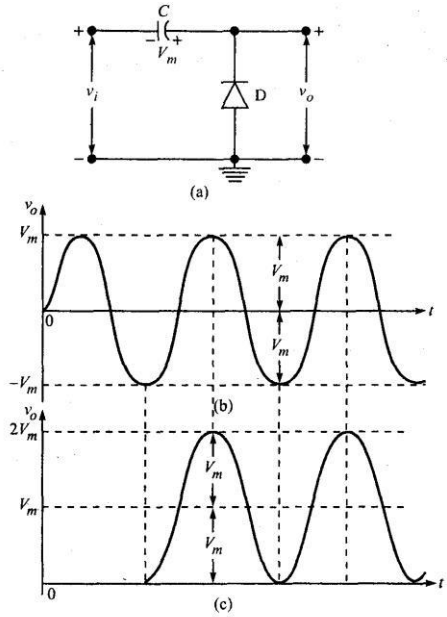


Figure 2.73 (a) A positive clamping circuit, (b) a sinusoidal input, and (c) a steady-state clamped output.

Let the input voltage be $v_i = V_m \sin$ *(ot* as shown in Figure 2.73(b). When v, goes negative, the diode gets forward biased and conducts and in a few cycles the capacitor gets charged to V_m with the polarity shown in Figure 2.73(a). Under steady-state conditions, the capacitor acts as a constant voltage source and the output is $v_o = v_i - (-V_m) = v_i + V_m$.

Based on the above relation between v_0 and v,, the output voltage waveform is plotted. As seen in Figure 2.73(c) the negative peaks of the input signal are clamped to zero level. Peak-to-peak value of output voltage = peak-to-peak value of input voltage = $2V_m$. There is no distortion of waveform. To accommodate for variations in amplitude of input, the diode D is shunted with a resistor as shown in Figure 2.74(a). When the amplitude of the input waveform is reduced, the output will adjust to its new value as shown in Figure 2.74(b).

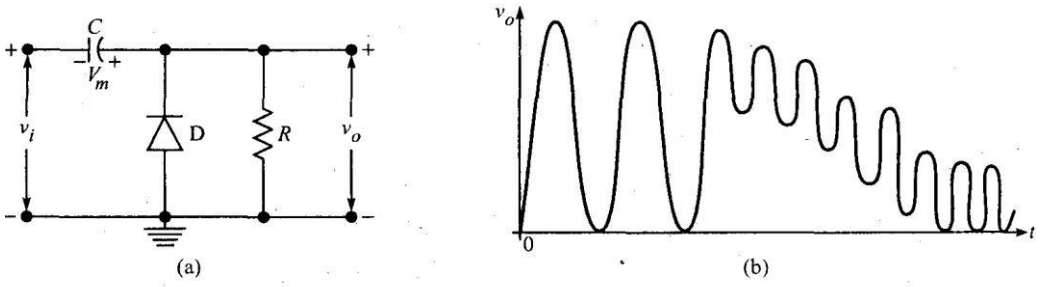


Figure 2.74 (a) Clamping circuit with a resistor R across D and (b) output during transient period.

Biased Clamping

If a voltage source of V_R volts is connected in series with the diode of a clamping circuit, the input waveform will be clamped with reference to V_R. Depending on the position of the diode, the input waveform may be positively clamped with reference to V_R, or negatively clamped with reference to V_R.

Clamping Circuit Taking Source and Diode Resistances Into Account

In the discussion of the clamping circuit of Figure 2.71, we neglected the output resistance of the source as well as the diode forward resistance. Many times these resistances cannot be neglected. Figure 2.79 shows a more realistic clamping circuit taking into consideration the output resistance of the source R_S, which may be negligible or may range up to many thousands of ohms depending on the source, and the diode forward resistance Rf which may range from tens to hundreds of ohms. Assume that the diode break point V_y occurs at zero voltage.

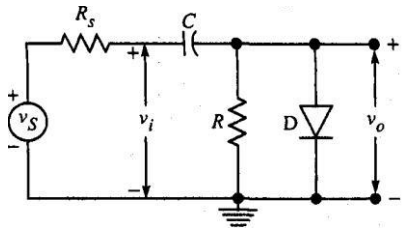


Figure 2.79 Clamping circuit considering the source resistance and the diode forward resistance.

The precision of operation of the circuit depends on the condition that $R \gg Rf$, and $R_r \gg R$. When the input is positive, the diode is ON and the equivalent circuit shown in Figure 2.80(a) results. When the input is negative, the diode is *OFF* and the equivalent circuit shown in Figure 2.80(b) results.

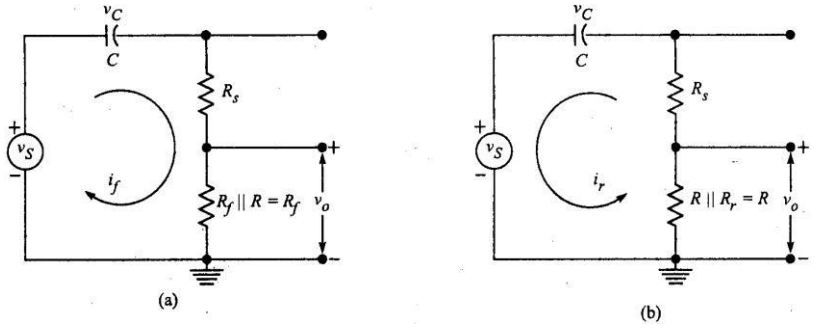


Figure 2.80 (a) Equivalent circuit when the diode is conducting and (b) the equivalent circuit when the diode is not conducting.

The transient waveform

When a signal is suddenly applied to the circuit shown in Figure 2.79 the capacitor charges (transient period) and gradually the steady-state condition is reached in which the positive peaks will be clamped to zero. The equivalent circuits shown in Figures 2.80(a) and 2.80(b) may be used to calculate the transient response.

Relation between tilts in forward and reverse directions

The steady-state output waveform for a square wave input. Consider that the square wave input shown in Figure 2.82(a) is applied to the clamping circuit shown in Figure 2.79. The general form of the output waveform would be as shown in Figure 2.82(b), extending in both positive and negative directions and is determined by the voltages V_1, V_2, V_1^1, and V'_2. These voltages may be calculated as discussed below.

In the interval $0 < t < T$, the input is at its higher level; so the diode is ON and the capacitor charges with a time constant $(R_S + R_f)C$, and the output decays towards zero with the same time constant. Hence, $V'_1 = V_1 e^{-T_1/(R_f+R_S)C}$ ---------- (i)

In the interval $T_1 < t < T_1 + T_2$, the input is at its lower level; so the diode is OFF and the capacitor discharges with a time constant $(R + R_S)C$, and the output rises towards zero with the same time constant. Hence $V'_2 = V_2 e^{-T_2/(R+R_S)C}$ ---------(ii)

Considering the conditions at t= 0. At $t = 0\sim$, $v_S = V''$, $v_0 = V_2$, the diode D is OFF and the equivalent circuit of Figure 2.80(b) results. The voltage across the capacitor is given by

$$v_C = V'' - \frac{V_2'}{R}(R + R_S) \quad \text{---------(iii)}$$

At $t = 0^+$, the input signal jumps to V, the output jumps to V_t, the diode conducts and the equivalent circuit of Figure 2.80(a) results. The voltage across the capacitor is given by

$$v_C = V' - \frac{V_1}{R_f}(R_f + R_S) \quad \text{----------(iv)}$$

Since the voltage across the capacitor cannot change instantaneously, equating equations (iii) and (iv), we have

$$V' - \frac{V_1(R_f + R_S)}{R_f} = V'' - \frac{V_2'(R + R_S)}{R} \quad \text{----------(v)}$$

$$V' - V'' = V = \frac{V_1(R_f + R_S)}{R_f} - \frac{V_2'(R + R_S)}{R}$$

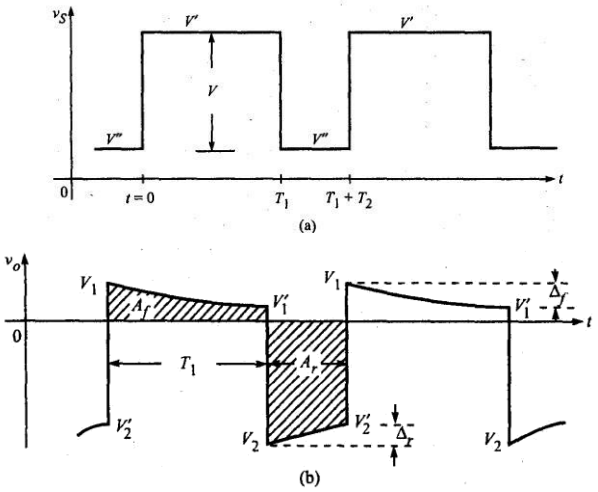


Figure 2.82 (a) A square wave input signal of peak-to-peak amplitude *V,* (b) the general form of the steady-state output of a clamping circuit with;' the input as in (a).

***Considering the conditions at t*= T_r.** At $t = T_r$, $v_S = V$, $v_0 = V_1$, the diode D is ON, and the equivalent circuit of Figure 2,80(a) results. The voltage across the capacitor is given by

$$v_C = V' - \frac{V_1'}{R_f}(R_f + R_S) \quad \text{----------(vi)}$$

At $t = T_r$, , $v_S = V'' = v_0 = V_2$, the diode D is OFF, and the equivalent circuit of Figure 2.80(b) results.

The voltage across the capacitor is given by

$$v_C = V'' - \frac{V_2}{R}(R + R_S) \quad \text{----------(vii)}$$

Since the voltage across the capacitor cannot change instantaneously, equating equations (vi) and (vii), we get

$$V' - \frac{V_1'(R_f + R_S)}{R_f} = V'' - \frac{V_2(R + R_S)}{R}$$

$$V' - V'' = V = \frac{V_1'(R_f + R_S)}{R_f} - \frac{V_2(R + R_S)}{R} \quad \text{----------(viii)}$$

From equations (i), (ii), (v) and (viii), the values V_1, V', V_2 and V_2' can be computed and the output waveform determined.

If the source impedance is taken into account, the output voltage jumps are smaller than the abrupt discontinuity V in the input. Only if $R_S = 0$, are the jumps in input and output voltages equal. Thus, when $R_S = 0$, $V_1 - V_2' = V_1' - V_2 = V$ Observe that the response is independent of the absolute levels V' and V'' of the input signal and is determined only by the amplitude V. It is possible, for example, for V'' to be negative or even for both V and V'' to be negative.
The average level of the input plays no role in determining the steady-state output waveform.

Under steady-state conditions, there is a tilt in the output waveform in both positive and negative directions. The relation between the tilts can be obtained by subtracting Eq. (viii) from Eq. (v), i.e.

$$\frac{R_f + R_S}{R_f}(V_1 - V_1') - \frac{R + R_S}{R}(V_2' - V_2) = 0$$

Where,

$V_1 - V_1' = \Delta_f$ = tilt in the forward direction
$V_2' - V_2 = \Delta_r$ = tilt in the reverse direction

$$\therefore \quad \Delta_f = \frac{R_f}{R_f + R_S} \times \frac{R + R_S}{R} \Delta_r$$

Since R_S is usually much smaller than R, then, the tilt in the forward direction Ay is almost always less than the tilt A_r in the reverse direction. Only when $R_S \ll R_f$, are the two tilts almost equal.

Clamping Circuit Theorem

Under steady-state conditions, for any input waveform, the shape of the output waveform of a clamping circuit is fixed and also the area in the forward direction (when the diode conducts) and the area in the reverse direction (when the diode does not conduct) are related.

The clamping circuit theorem states that, for any input waveform under steady-state conditions, the ratio of the area *Af* ***under the output voltage curve in the forward direction to that in the reverse direction*** A_r ***is equal to the ratio R//R-***

This theorem applies quite generally independent of the input waveform and the magnitude of the source resistance. The proof is as follows:

Consider the clamping circuit of Figure 2.79, the equivalent circuits in Figures 2.80(a) and 2.80(b), and the input and output waveforms of Figures 2.82(a) and 2.82(b) respectively.

In the interval $0 < t < T$, the input is at its upper level, the diode is ON, and the equivalent circuit of Figure 2.80(a) results. If v/(f) is the output waveform in the forward direction, then the capacitor charging current is $i_f(t) = \frac{v_f(t)}{R_f}$ Therefore, -the charge gained by the capacitor during the forward interval is

$$Q_g = \int_0^{T_1} i_f(t)dt = \frac{1}{R_f}\int_0^{T_1} v_f(t)dt = \frac{A_f}{R_f}$$

In the interval TJ $< t < T_{\{} + T_2$, the input is at its lower level, the diode is OFF, and the equivalent circuit of Figure 2.80(b) results. If $v_r(t)$ is the output voltage in the reverse direction, then the current which discharges the capacitor is $i_r(t) = \frac{v_r(t)}{R}$

Therefore, the charge lost by the capacitor during the reverse interval is

$$Q_l = \int_{T_1}^{T_1+T_2} i_r(t)\,dt = \frac{1}{R}\int_{T_1}^{T_1+T_2} v_r(t)dt = \frac{A_r}{R}$$

Under steady-state conditions, the net charge acquired by the capacitor over one cycle must be equal to zero. Therefore, the charge gained in the interval $0 < t < T_{\}}$, will be equal to the charge lost in the interval $T_1 < t < T_1 + T_2$, i.e. Q_g = Ql

$$\frac{A_f}{R_f} = \frac{A_r}{R} \qquad \text{i.e.} \qquad \frac{A_f}{A_r} = \frac{R_f}{R}$$

UNIT – III

MULTIVIBRATORS

Transistor as a switch, transistor-switching times. Analysis and Design of Bistable, Monostable, Astable Multivibrators and Schmitt trigger using transistors.

JUNCTION DIODE—SWITCHING TIMES

Diode forward recovery time

When a diode is driven from the: reverse-biased condition to the forward-biased condition or in the opposite direction, the diode response is accompanied by a transient, and an interval of time elapses before the diode recovers to its steady state. The nature of the forward recovery transient depends on the magnitude of the current being driven through the diode and the rise time of the driving signal.

Consider the voltage which develops across the diode when the input is a current source supplying a step current I_V as shown in Figure 3,1 (a). If the current amplitude is comparable to or larger than the diode rated current, and if the rise time of the current step is small enough, then the waveform of the voltage which appears across the diode is shown in Figure 3.1(b). The overshoot results from the fact that initially the diode acts not as a p-n junction diffusion device but as a resistor, tn the steady-state condition, the current which flows through the diode is a diffusion current which results from the gradient in the density of minority carriers. If the current is large enough, then there will also be an ohmic drop across the diode. The ohmic drop is initially very large, for immediately after the application of the current, the holes, say, will npn have time to diffuse very far into the n-side in order to build up a minority carrier density. Therefore except near the junction, there will be no minority charge to establish a density gradient, and the current flow through the mechanism of diffusion will not be possible. Indeed, an electric field will be required to achieve current flow by exerting force on the majority carriers. This electric field gives rise to the ohmic drop. With the passage of time, however, the ohmic drop will decrease as more and more minority carriers become available from the junction, and current by diffusion takes over.

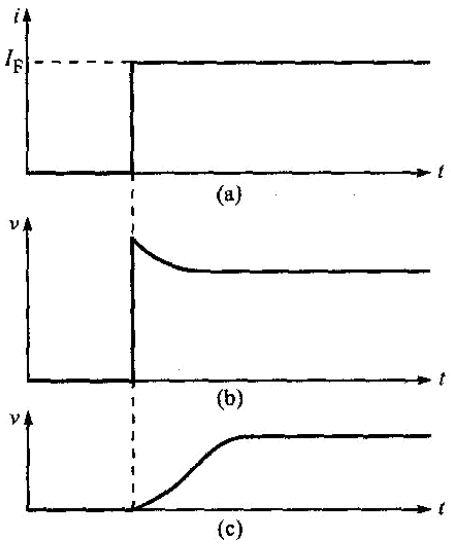


Figure 3.1(aj Input step current to a diode, (b) diode voltage when the current is large, arid (c) diode voltage when the current is small.

The magnitude of the overshoot will increase as the magnitude of the input current increases. At large current amplitudes, the diode behaves as a combination of a resistor and an inductor. At low currents the diode is representable by a parallel resistor-capacitor combination. At intermediate currents, the diode behaves as a resistor, inductor, and capacitor circuit and oscillations may be produced.

The forward recovery time f_{fr}, for a specified rise time of the input current is the time difference between the 10% point of the diode voltage and the time when this voltage reaches and remains within 10% of its final value. The forward recovery time does not usually constitute a serious problem.

Diode reverse recovery time

When an external voltage is impressed across a junction in the direction that reverse biases it, very little current called the reverse saturation current flows. This current is because of the minority carriers.

The density of minority carriers in the neighbourhood of the junction in the steady state is shown in Figure 3.2(a). Here the levels $p_{nl)}$ and n are the thermal equilibrium values of the minority carrier densities on the two sides of the junction in the absence of an externally impressed voltage. When a reverse voltage is applied, the density of minority carriers is shown by the solid Sines marked p_n and n_p. Away from the junction, the minority carrier density remains unaltered, but as these carriers approach the junction they are rapidly swept across and the density of minority carriers diminishes to zero at the junction. The reverse saturation current which flows is small because the density of thermally generated minority carriers is very small.

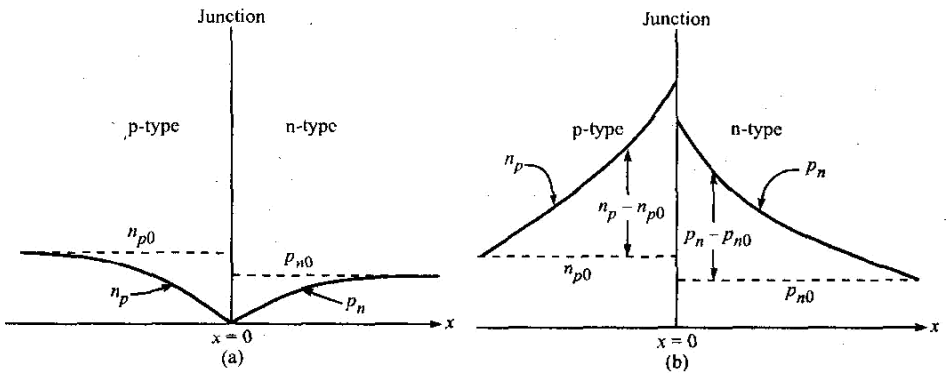


Figure 3.2 Minority-carrier density distribution as a function of the distance *x* from a junction; (a) a reverse-biased junction and (b) a forward-biased junction.

When the external voltage forward biases the junction, the steady-state density of minority carriers is as shown in Figure 3.2(b). The injected or excess hole density is *(p_n - p_{nQ})* and the excess electron density is *(n_p - n_{pQ}).*

In a diode circuit which has been carrying current in the forward direction, if the external voltage is suddenly reversed, the diode current will not immediately fall to its steady-state reverse value. The current cannot attain its steady-state value until the minority carrier distribution changes the form in Figure 3.2(b) to the distribution shown in Figure 3.2(a). Until such time as the injected or excess minority carrier density p_n - p_{nQ} (or n_p -n_{p0}) drops nominally to zero, the diode will continue to conduct easily and the current will be determined by the external resistance in the diode circuit.

Storage and transition times

The sequence of events which occurs when a conducting diode is reverse biased is shown in Figure 3.3. The input voltage shown in Figure 3.3(b) is applied to a diode circuit shown in Figure 3.3(a). Up to *t* = *t*\, v, = V_f. The resistance R_L is assumed large so that the drop across R_L is large compared with the drop across the diode.

$$i \approx \frac{V_F}{R_L} = I_F$$

At the time *t* ~ *t*[, the input voltage reverses abruptly to the value V; = - VR, the current reverses, $i \approx \frac{-V_R}{\sim} = -I_R$ until the time *t* - t_2. At *t* ~ *t*^ as shown in Figure 3.3(c), the injected minority carrier density at the junction drops to zero, that is, the minority carrier density reaches its equilibrium state. If the diode ohmic resistance is R_A, then at time *t*\, the diode voltage falls slightly by [(VF + VR)] but does not reverse as shown in Figure 3.3(e). At *t* = ?2 when the excess minority carriers in the immediate neighbourhood of the junction have been swept back across the junction, the diode

voltage begins to reverse as shown in Figure 3.3(e) and the magnitude of the diode current begins to decrease as shown in Figure 3.3(d). The interval from t\ to t_2 for the minority charge to become zero is called the *storage time* t_s. The time which elapses between r_2 and the time when the diode has nominally recovered is called the *transition time* t_t. The recovery interval will be completed when the minority carriers which are at some distance from the junction have diffused to the junction, crossed it and then, in addition, the junction transition capacitance across the reverse-biased junction has charged through R_L to the voltage $-V_R$ as shown in Figure 3.3(e).

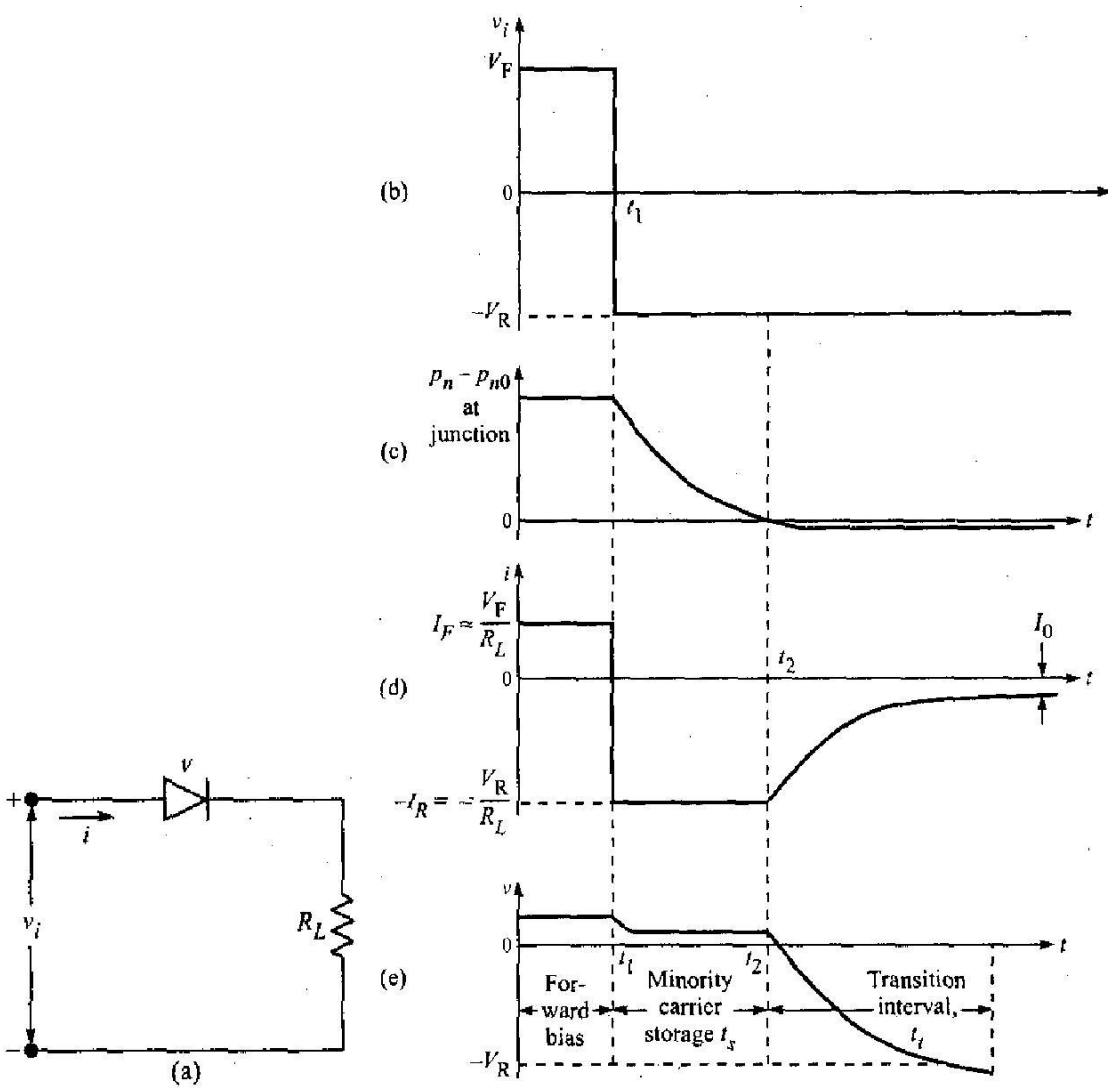


Figure 3.3 The waveform in (b) is applied to the diode circuit in (a), (c) the excess carrier density at the junction, (d) the diode current, and (e) the diode voltage.

PIECE-WISE LINEAR DIODE CHARACTERISTICS

A large-signal approximation which often leads to a sufficiently accurate engineering solution is the piece-wise linear representation. The piece-wise linear approximation for a semiconductor diode characteristic is shown in Figure 3.4. The breakdown is at V_y, which is

called the *offset* or *threshold* voltage. The diode behaves like an open-circuit if $v < V_r$ The characteristic shows a constant incremental resistance $r = dv/di$ if $v > V_r$ Here r is called the forward resistance. The static resistance $R_f = V_\gamma$ is not constant and is not useful.

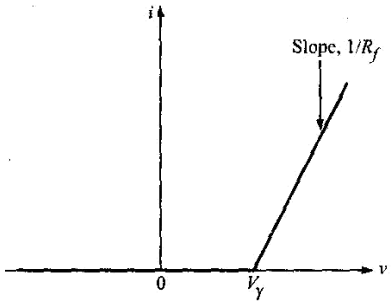


Figure 3.4 The piece-wise linear characteristic of a diode.

The numerical values of V_γ and R_f to be used depend upon the type of diode and the contemplated voltage and current swings. Typically: For current swings from cut-off to 10 mA

For Ge, $V_\gamma = 0.2$ V and $R_f = 20\ \Omega$
For Si, $V_\gamma = 0.6$ V and $R_f = 15\ \Omega$

For current swings up to 50 mA

For Ge, $V_\gamma = 0.3$ V and $R_f = 6\ \Omega$
For Si, $V_\gamma = 0.65$ V and $R_f = 5.5\ \Omega$

TRANSISTOR AS A SWITCH

A transistor can be used as a switch. It has three regions of operation. When both emitter^ base and collector-base junctions are reverse biased, the transistor operates in the cut-o! region and it acts as an open switch. When the emitter base junction is forward biased and the collector base junction is reverse biased, it operates in the active region and acts as auf amplifier. When both the emitter-base and collector-base junctions are forward biased, it! operates in the saturation region and acts as a closed switch. When the transistor is switched! from cut-off to saturation and from saturation to cut-off with negligible active region, thej transistor is operated as a switch. When the transistor is in saturation, junction voltages are'i very small but the operating currents are large. When the transistor is in cut-off, the currents* are zero (except small leakage current) but the junction voltages are large.

In Figure 3.6 the transistor Q can be used to connect and disconnect the load R_L from the source Vcc When Q is saturated it is like a closed switch from collector to emitter and when Q is cut-off it is like an open switch from collector to emitter.

$$I_C = \frac{V_{CC} - V_{CE}}{R_L} \quad \text{and} \quad I_B = \frac{V_{BB} - V_{BE}}{R_B}$$

Referring to the output characteristics shown in Figure 3.6(b), the region below the I_B = 0 curve is the cut-off region. The intersection of the load line with $I_B = 0$ curve is the *cut-off point.* At this point, the base current is zero and the collector current is negligible. The emitter diode comes out of forward bias and the normal transistor action is lost, i.e, V_{CE}(cut-off) = V_{CC}. The transistor appears like an open switch.

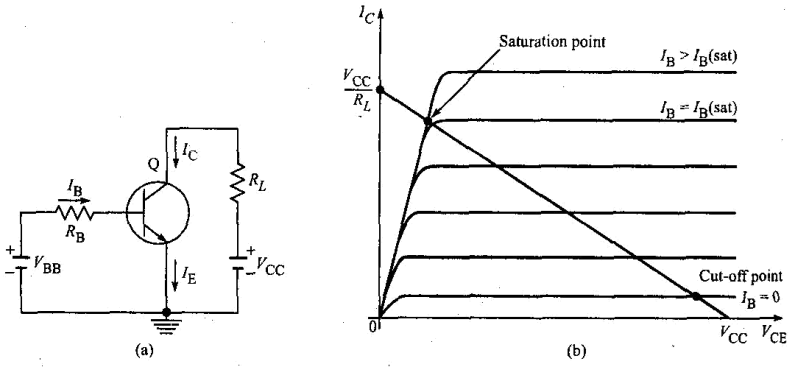


Figure 3.6 (a) Transistor used as a switch and (b) output characteristics with load line (dc).

The intersection of the load line with the I_B - Ie(sat) curve is called the *saturation point.* At this point, the base current is I_B(sat) and the collector current is maximum. 'At saturation, the collector diode comes out of cut-off and again the normal transistor action is lost, i.e. Ic(sat) = *Vcc/R_L.Ie*(sat) represents the minimum base current required to bring the transistor into saturation. For $0 < I_B < I_B$(sat), the transistor operates in the active region. If the base current is greater than I_B(sat), the collector current approximately equals V_{CC}/IC and the transistor appears like a closed switch.

TRANSISTOR SWITCHING TIMES

When the transistor acts as a switch, it is either in cut-off or in saturation. To consider the behaviour of the transistor as it makes transition from one state to the other, consider the circuit shown in Figure 3,7(a) driven by the pulse waveform shown in Figure 3.7(b). The pulse waveform makes transitions between the voltage levels V_2 and V_1. At V_2 the transistor is at cut-off and at V the transistor is in saturation. The input waveform v; is applied between the base and the emitter through a resistor *R_B.*

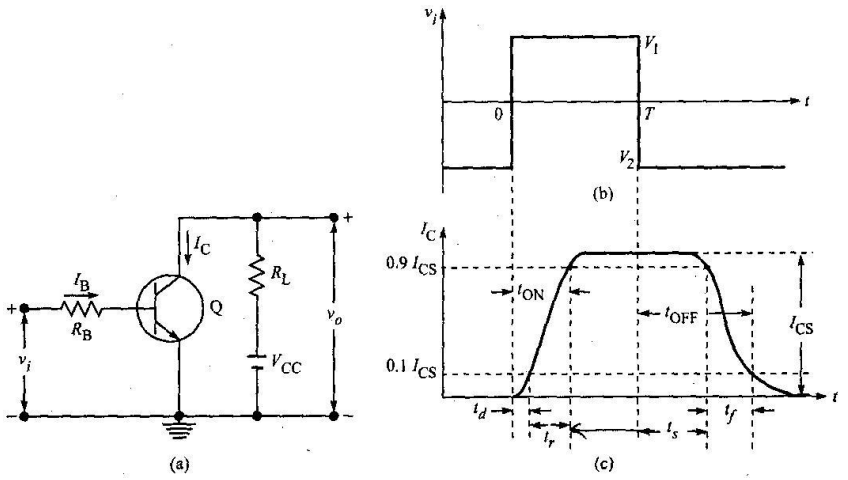


Figure 3.7 (a) Transistor as a switch, (b) input waveform, and (c) the response of collector current versus time.

The response of the collector current ic to the input waveform, together with its time relationship to the waveform is shown in Figure 3.7(c), The collector current does not immediately respond to the input signal. Instead there is a delay, and the time that elapses during this delay, together with the time required for the current to rise to 10% of its maximum (saturation) value (I_{Cs} = Vcc/Rc) is called the delay time t_d. The current waveform has a nonzero rise time f_r, which is the rise time required for the current to rise from 10% to 90% of Ics- The total turn-on time T_{ON} is the sum of the *delay time* and the rise time, i.e. $T_{ON} = t_d + t_r$. When the input signal returns to its initial state, the collector current again fails to respond immediately. The interval which elapses between the transition of the input waveform and the time when /c has dropped to 90% of /cs is called the *storage time* t_s. The storage interval is followed by the fall time ly, which is the time required for 7C to fall from 90% to 10% of Ics- The turn-off time ^OFF is defined as the sum of the storage and fall times, i.e. $T_{OFF} = t_r + t_f$ We shall now consider the physical reasons for the existence of each of these times.

The delay time

There are three factors that contribute to the delay time. First there is a delay which results from the fact that, when the driving signal is applied to the transistor input, a non-zero time is required to charge up the junction capacitance so that the transistor may be brought, from cut-off to the active region. Second, even when the transistor has been brought to the point where minority carriers have begun to cross the emitter junction into the base, a nonzero time is required before these carriers can cross the base region to the collector junction and be recorded as collector current. Finally, a nonzero time is required before the collector current can rise to

10% of its maximum value. Rise time and fall time The rise time and fall time are due to the fact that, if a base current step is used to saturate the transistor or to return it from saturation into cut-off, the collector current must traverse the active region. The collector current increases or decreases along an exponential curve. Storage time The failure of the transistor to respond to the trailing edge of the driving pulse for the time interval t_s, results from the fact that a transistor in saturation has a saturation charge of excess minority carriers stored in the base. The transistor cannot respond until the saturation excess charge has been removed.

MULTIVIBRATORS

Multi means many; *vibrator* means oscillator. A circuit which can oscillate at a number of frequencies is called a *multivibrator*. Basically there are three types of multivibrators:

1. Bistable multivibrator
2. Monostable multivibrator
3. Astable multivibrator

Each of these multivibrators has two states. As the names indicate, a bistable multivibrator has got two stable states, a monostable multivibrator has got only one stable state (the other state being quasi stable) and the astable multivibrator has got no stable state (both the states being quasi stable). The stable state of a multivibrator is the state in which the device can stay permanently. Only when a proper external triggering signal is applied, it will change its state. Quasi stable state means temporarily stable state. The device cannot stay permanently in this state. After a predetermined time, the device will automatically come out of the quasi stable state.

In this chapter we will discuss multivibrators with two-stage regenerative amplifiers. They have two cross-coupled inverters, i.e. the output of the first stage is coupled to the input of the second stage and the output of the second stage is coupled to the input of the first stage. In bistable circuits both the coupling elements are resistors (i.e. both are dc couplings). In monostable circuits, one coupling element is a capacitor (ac coupling) and the other coupling element is a resistor (dc coupling) In astable multivibrators both the coupling elements are capacitors (i.e. both are ac couplings).

A bistable multivibrator requires a triggering signal to change from one stable state to another. It requires another triggering signal for the reverse transition. A monostable multivibrator requires a triggering signal to change from the stable state to the quasi stable state but no triggering signal is required for the reverse transition, i.e. to bring it from the quasi stable state to the stable state. The astable multivibrator does not require any triggering signal at all. It

keeps changing from one quasi stable state to another quasi stable state on its own the moment it is connected to the supply.

A bistable multivibrator is the basic memory element. It is used to perform many digital operations such as counting and storing of binary data. It also finds extensive applications in the generation and processing of pulse type waveforms. The monostable multivibrator finds extensive applications in pulse circuits. Mostly it is used as a gating circuit or a delay circuit. The astable circuit is used as a master oscillator to generate square waves. It is often a basic source of fast waveforms. It is a free running oscillator. It is called a *square wave generator.* It is also termed a *relaxation oscillator.*

BISTABLE MULTIVIBRATOR

A bistable multivibrator is a multivibrator which can exist indefinitely in either of its two stable states and which can be induced to make an abrupt transition from one state to the other by means of external excitation. In a bistable multivibrator both the coupling elements are resistors (dc coupling). The bistable multivibrator is also called a multi, Eccles-Jordan circuit (after its inventors), trigger circuit, scale-of-two toggle circuit, flip-flop, and binary. There are two types of bistable multivibrators:

1. Collector coupled bistable multivibrator
2. Emitter coupled bistable multivibrator

There are two types of collector-coupled bistable multivibrators:

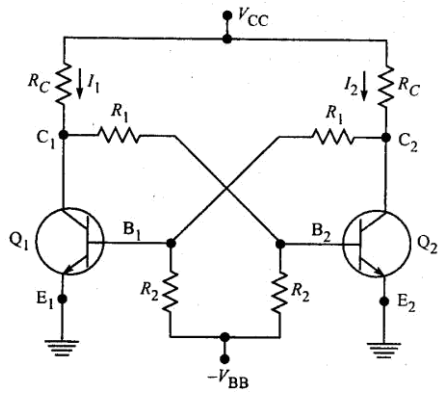
1. Fixed-bias bistable multivibrator
2. Self-bias bistable multivibrator

A FIXED-BIAS BISTABLE MULTIVIBRATOR

Figure 4.1 shows the circuit diagram of a fixed-bias bistable multivibrator using transistors (inverters). Note, that the output of each amplifier is direct coupled to the input of the other amplifier. In one of the stable states, transistor Q[is ON (i.e. in saturation) and Q_2 is OFF (i.e. in cut-off), and in the other stable state Qj is OFF and Q_2 is ON. Even though the circuit is symmetrical, it is not possible for the circuit to remain in a stable state with both the transistors conducting (i.e. both operating in the active region) simultaneously and carrying equal currents. The reason is that if we assume that both the transistors are biased equally and are carrying equal currents /[and 7_2 and suppose there is a minute fluctuation in the current *1*\~—let us say it increases by a small amount—then the voltage at the collector of Qi decreases. This will result in a decrease in voltage at the base of Q_2. So Q_2 conducts less and $/_2$ decreases and hence the

potential at the collector of Q_2 increases. This results in an increase in the base potential of *Qi.* So, Qi conducts still more and /[is further increased and the potential at the collector of Q_t is further reduced, and so on. So, the current *I*\ keeps on increasing and the current $/_2$ keeps on decreasing till $Q_($ goes into saturation and Q_2 goes into cut-off. This action takes place because of the regenerative feedback incorporated into the circuit and will occur only if the loop gain is greater than one.*A stable state of a binary is one in which the voltages and currents satisfy the Kirchhoff's laws and are consistent with the device characteristics and in which, in addition, the condition of the loop gain being less than unity is satisfied.*

The condition with respect to loop gain will certainly be satisfied, if either of the two devices is below cut-off or if either device is in saturation. But normally the circuit is designed such that in a stable state one transistor is in saturation and the other one is ir cut-off, because if one transistor is biased to be in cut-off and the other one to be in active region, as the temperature changes or the devices age and the device parameters vary, the quiescent point changes and the quiescent output voltage may also change appreciably Sometimes the drift may be so much that the device operating in the active region may gc into cut-off, and with both the devices in cut-off the circuit will be useless.



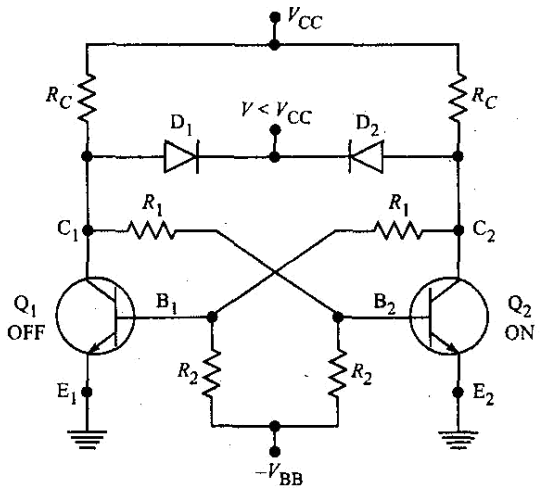
Selection of components in the fixed-bias bistable multivibrator

In the fixed-bias binary shown in Figure 4.1., nearly the full supply voltage V_{CC} will appear across the transistor that is OFF. Since this supply voltage V_{cc} is to be reasonably smaller than the collector breakdown voltage SVce. *Vcc* $*^S$ restricted to a maximum of a few tens of volts. Under saturation conditions the collector current I_C is maximum. Hence *RC* must be chosen so that this value of 7_C (= VCC/^G) does ^{not} exceed the maximum permissible limit. The

values of R\, /?2 and V_{BB} must be selected such that in one stat>le state the base current is large enough to drive the transistor into saturation whereas in the second stable state the emitter junction must be below cut-off. The signal at a collector called the output swing V_w is the change in collector voltage resulting from a transistor going from one state to the other, i.e. $V_w = V_{Ci} - ^C2-$ If the loading caused by RI can be neglected, then the collector voltage of the OFF transistor is V_{cc}. Since the collector saturation voltage is few tenths of a volt, then the swing $V_w = V_{cc}$, independently of RQ- The component values, the supply voltages and the values of $/_{CBO}$, $h^{\wedge}$, $V_{BE}(sat)$, and $V_{CE}(sat)$ are sufficient for the analysis of transistor binary circuits.

Loading

The bistable multivibrator may be used to drive other circuits and hence at one or both the collectors there are shunting loads, which are not shown in Figure 4.1. These loads reduce the magnitude of the collector voltage V_{C1} of the OFF transistor. This will result in reduction of the output voltage swing. A reduced $V_{C[}$ will decrease 7_{B2} and it is possible that Q_2 may not be driven into saturation- Hence the flip-flop circuit components must be chosen such that under the heaviest load, which the binary drives, one- transistor remains in saturation while the other is in cut-off. Since the resistor R_l also loads the OFF transistor, to reduce loading, the value of $R]$ should be as large as possible compared to the value of R_c. But to ensure a loop gain in excess of unity during the transition between the states, $R^{\wedge}$ should be selected such that For some applications, the loading varies with the operation being performed. In such cases, the extent to which a transistor is driven into saturation is variable. A constant output swing V\v = V, arid a constant base saturation current I_{B2} can be obtained by clamping the collectors to an auxiliary voltage $V < V_{cc}$ through the diodes DI and D_2 as indicated in Figure 4.2. As Qi cuts OFF, its collector voltage rises and when it reaches V, the "collector catching diode" D| conducts and clamps the output to V.



Transistor as an ON-OFF switch

In digital circuits transistors operate either in the cut-off region or in the saturation region. Specially designed transistors called switching transistors with negligible active region are used. In the cut-off region the transistor does not conduct and acts as a open switch. In the saturation region the transistor conducts heavily and acts as a closed switch-In a binary which uses two cross-coupled transistors, each of the transistors is alternately cut-off and driven into saturation. Because of regenerative feedback provided both the transistors cannot be.ON or both cannot be OFF simultaneously. When one transistor is ON, the other is OFF and vice versa.

Standard specifications

In the cut-off region, i.e. for the OFF state

V_{BE} (cut-off) : ≤ 0 V for silicon transistor
≤ -0.1 V for germanium transistor

In the saturation region, i.e. for the ON state

V_{BE} (sat) : 0.7 V for silicon transistor
0.3 V for germanium transistor
V_{CE} (sat) : 0.3 V for silicon transistor
0.1 V for germanium transistor

The above values hold good for n-p-n transistors. For p-n-p transistors the above values with opposite sign are to be taken.

Test for saturation

To test whether a transistor is really in saturation or not evaluate the collector current i_C and the base current i_B independently.

If $i_B > i_B$ (min), where i_B (min) = i_C/h_{FE} (min) the transistor is really in saturation.
If $i_B \leq i_B$ (min), the transistor is not in saturation.

Test for cut-off

To test whether a transistor is really cut-off or not, find its base-to-emitter voltage. If V_{BE} is negative for an n-p-n transistor or positive for a p-n-p transistor, the transistor is really cut-off.

THE EMITTER-COUPLED BINARY (THE SCHMITT TRIGGER CIRCUIT)

Figure 4.29 shows the circuit diagram of an emitter-coupled bistable multivibrator using n-p-n transistors. Quite commonly it is called *Schmin trigger* after the inventor of its vacuum-tube version. It differs from the basic collector-coupled binary in that the coupling from the output of the second stage to the input of the first stage is missing and the feedback is obtained now through a common emitter resistor R_E. It is a bistable circuit and the existence of only two stable states results form the fact that positive feedback is incorporated into the circuit, and from the further fact that the loop gain of the circuit is greater than unity. There are several ways to adjust the loop gain. One way of adjusting the loop gain is.by varying /?$_{C1}$. Suppose R_C] is selected such that the loop gain is less than unity. When fl $_{cl}$ is small, regeneration is not possible.

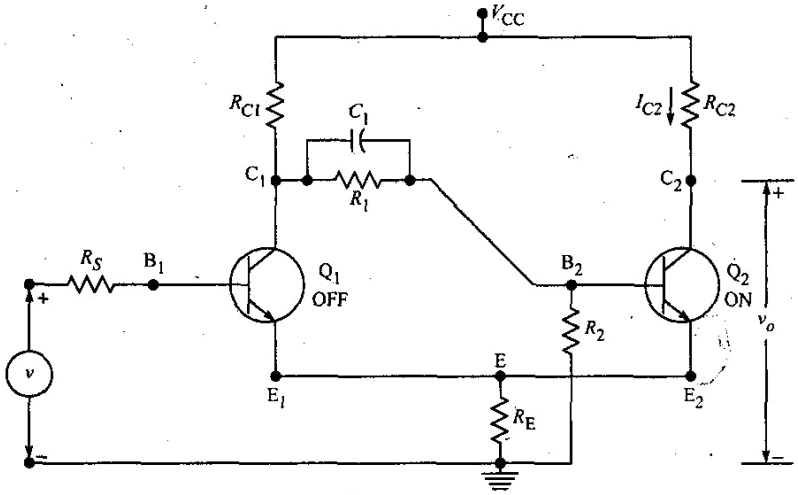


Figure 4.29 An emitter-coupled binary.

For the circuit of Figure 4.29, under quiescent conditions Qi is OFF and Q_2 is ON because it gets the required base drive from V_{CC} through R_C*i* and /?j. So the output voltage

$$v_o = V_{CC} - I_{C2}R_{C2} \qquad \text{(where } I_{C2} \text{ is the current in } R_{C2} \text{ when } Q_1 \text{ is OFF)}$$

is at its lower level. With Q_2 conducting, there will be a voltage drop across *RE* -7$_{B2}$)/?E> and this will elevate the emitter of *Q*\. As the input v is increased from zero, the circuit will not respond until Qi reaches the cut-in point (at v = V_t). Until then the output remains at its lower level. With Oj conducting (for v > V|) the circuit will amplify because Q_2 is already conducting and since the gain Av</Av is positive, the output will rise in response to the rise in input. As v continues to rise, C_t and hence B_2 continue to fall and E_2 continues to rise. Therefore a value of v will be reached at which Qa is turned OFF. At this point v_0 = V_{CC} and the output remains constant at this value of V_{cc}, even if the input is further increased. A plot of v_a versus v is shown in Figure 4.30(a) for loop gain < 1.

Suppose the loop gain is increased by increasing the resistance R_{ci}. Such a change will have negligible effect on the cut-in point V| of Qj. However in the region of amplification (i.e. for v > *V{)* the amplifier gain Av</Av will increase and so the slope of the rising portion of the plot in Figure 4.30(a) will be steeper. This increase in slope with increase in loop gain continues until at a loop gain of unity where the circuit has just become regenerative the slope will become infinite. And finally when the loop gain becomes greater than unity, the- slope becomes negative and the plot of v_a versus v assumes the S shape shown in Figure 4.30(b).

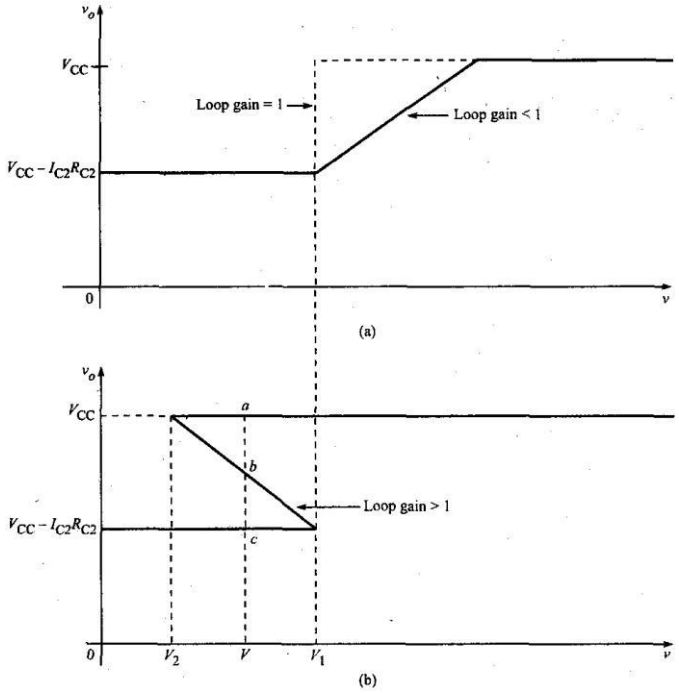


Figure 4.30 Response of emitter-coupled binary for (a) loop gain < 1 and (b) loop gain > 1.

The behaviour of the circuit may be described by using this S curve. As v rises from **zero** voltage, v_0 will remain at its lower level (= V_{CC} ~ 'c2 ^ca) ^{unt}*l ^{v} reaches *V*. (This value of v = V, at which the transistor **Qi** just enters into conduction is called the upper triggering point, UTP.) As v exceeds V_J the output will make an abrupt .transition to its higher level (= V_{cc}). For v > V_h **Qj** is ON and **Q_2** is **OFF.** Similarly if v is initially greater than V], then as v is decreased, the output will remain at its upper level until v attains a **definite** level V_2 at which point the circuit makes an abrupt transition to its lower level. For v < ^2> Qi is **OFF** and **Q2** is **ON.** (This value of v = V_2 at which the transistor **Q_2** resumes conduction is called the lower triggering point, LTP.) This circuit exhibits hysteresis, that is, to effect a transition in one direction we must first pass beyond the voltage at which the reverse transition took place.

A vertical line drawn at v = *V* which lies between V_2 and Vi intersects the S curve at three points *a, b* and *c.* The upper and lower points a and *c* are points of stable equilibrium.

The S curve is a plot of values which satisfy Kirchhoff's laws and which are consistent with the transistor characteristics. At v = V, the circuit will be at a or *c,* depending on the direction of approach of v towards

V. When v = V in the range between V_2 and V|, the Schmitt circuit is in one of its two possible stable states and hence is a bistable circuit.

Applications of Schmitt trigger circuit

Schmitt trigger is also a bistable multivibrator. Hence it can be used in applications where a normal binary is used. However for applications where the circuit is to be triggered back-and-forth between stable states, the normal binary is preferred because of its symmetry. Since the base of Q] is not involved in regenerative switching, the Schmitt trigger is preferred for applications in which the advantage of this free terminal can be taken. The resistance K_{C2} $^{m\ me}$ output circuit of Q_2 is not required for the operation of the binary. Hence this resistance may be selected over a wide range to obtain different output signal amplitudes.

A most important application of the Schmitt trigger is its use as an amplitude comparator to mark the instant at which an arbitrary waveform attains a particular reference level. As input v rises to Vi or falls to V_2, the circuit makes a fast regenerative transfer to its other state.

Another important application of the Schmitt trigger is as a squaring circuit. It can convert a sine wave into a square wave. In fact, any slowly varying input waveform can be converted into a square wave with faster leading and trailing edges as shown in Figure 4.31, if the input has large enough excursions to carry the input beyond the limits of the hysteresis range, $V_H = V\backslash - V_2$.

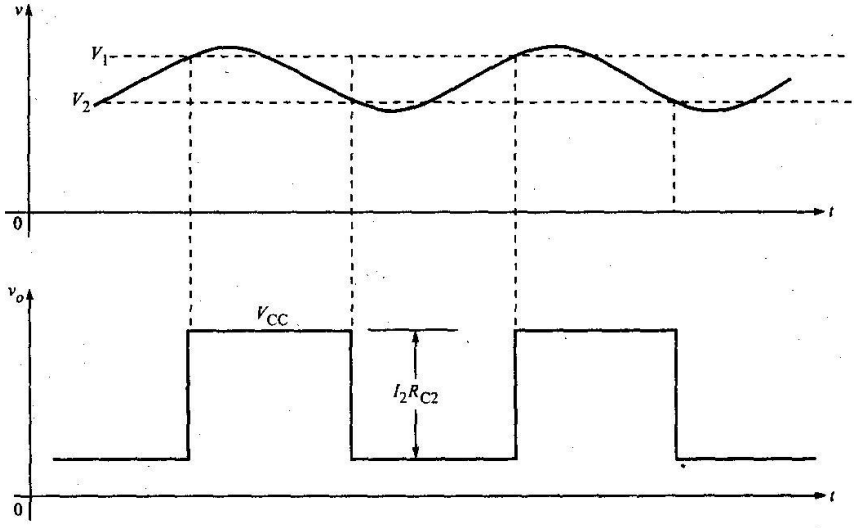


Figure 4.31 Response of the emitter-coupled binary to an arbitrary input waveform.

In another important application, the Schmitt trigger circuit is triggered between its two stable states by alternate positive and negative pulses. If the input is biased at a voltage *V* between V_2 and $V\backslash$ and if a positive pulse of amplitude greater than $V\backslash - V$ is coupled to the input, then Qj will conduct and Q_2 will be OFF. If now a negative pulse of amplitude larger than $V - V_2$ is coupled to the input, the circuit will be triggered back to the state where Qj is OFF and Q_2 is ON.

Hysteresis

If the amplitude of the periodic input signal is large compared with the hysteresis range V_H, then the hysteresis of the Schmitt trigger is not a matter of concern. In some applications, a large hysteresis range will not allow the circuit to function properly.

Hysteresis may be eliminated by adjusting the loop gain of the circuit to unity. Such an adjustment may be made in a number of ways:

(1) The loop gain may be increased or decreased by increasing or decreasing the resistance ^ci-

(2) The loop gain may be increased or decreased by adding a resistance /?$_{E1}$ in series with the emitter of Qi, or by adding a resistance 7?^ in series with the emitter of Q_2 and then decreasing or increasing R_{El} and R_{E2}. Since /?$_{C1}$ and R_{EJ} are in series with Qi, these resistors will have no effect on the circuit when Qi is OFF. Therefore, these resistors will not change V\ but may be used to move V_2 closer to or coincident with V\. Similarly, R_{E2} will affect V\ but not V_2.

(3) The loop gain may also be varied by varying the ratio $R[/(Ri + /?_2)$. Such an adjustment will change both V\ and V_2.

(4) The loop gain may be increased by increasing the value of $R$$.

If /?$_{E1}$ or R_{E2} is larger than the value required to give zero hysteresis, then the gain will be less than unity and the circuit will not change state. So, usually R_E\ or /?$_{E2}$ is chosen so that a small amount of hysteresis remains in order to ensure that the loop gain is greater than unity.

Vi is independent of R_s but V_2 depends on $R$$ and increases with an increase in the value of R_s. So for a large value of R_s it is possible for V_2 to be equal to V\, Hysteresis is thus eliminated and the gain is unity. If R_s exceeds this critical value, the loop gain falls below unity and the circuit cannot bs triggered. If R_s is too small, the speed of operation of the circuit is reduced.

Derivation of expression for UTP

The upper triggering point UTP is defined as the input voltage V_l at which the transistor Qi just enters into conduction. To calculate V_b we have to first find the current in Q_2 when Q! just enters into conduction. For this we have to find the Thevenin's equivalent voltage V and the Thevenin's equivalent resistance tf$_B$ at the base of Q_2, where

$$V' = V_{CC}\frac{R_2}{R_2 + R_{C1} + R_1} \quad \text{and} \quad R_B = R_2 \parallel (R_{C1} + R_1) = \frac{R_2 (R_{C1} + R_1)}{R_2 + R_{C1} + R_1}$$

It is possible for Q2 to be in its active region or to be in saturation. Assuming that Q_2 is in its active region

$$I_{C2} = h_{FE} I_{B2} \qquad \therefore I_{E2} = I_{C2} + I_{B2} = (h_{FE} + 1) I_{B2}$$

In the circuit shown in Figure 4.32, to calculate V_1, we replace V_{CC}, KCI> ^i anc* ^2 of Figure 4.29 by V' and R_B at the base of Q_2.

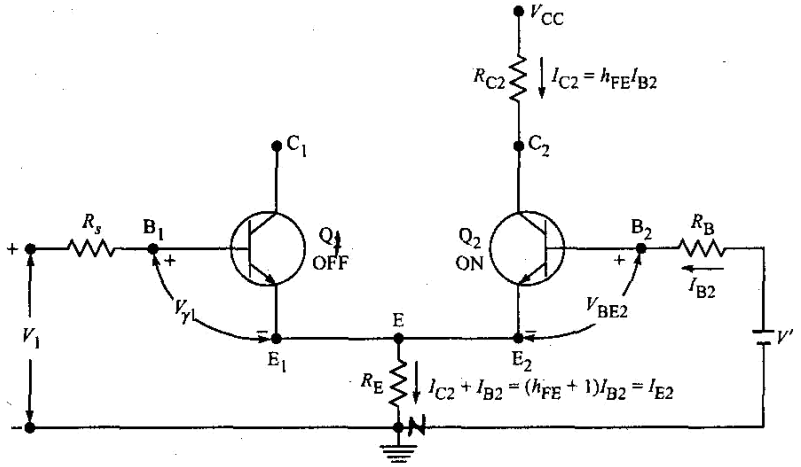


Figure 4.32 The equivalent circuit of Figure 4.29 with Q| just at cut-in.

Writing KVL around the base loop of Q_2,

$$V' - I_{B2}R_B - V_{BE2} - I_{B2}(h_{FE} + 1)R_E = 0$$

$$\therefore \quad I_{B2} = \frac{V' - V_{BE2}}{(h_{FE} + 1)R_E + R_B}$$

Hence $$V_{EN} = I_{B2}(h_{FE} + 1)\, R_E = \frac{(V' - V_{BE2})\,(h_{FE} + 1)\, R_E}{R_B + R_E\,(h_{FE} + 1)}$$

Also $$V_{EN1} = V_{EN} = V_{EN2}$$

Since Q_1 is just at cut-in, $I_{B1} = 0$ and $V_{BE1} = V_{\gamma 1}$

$$\therefore \quad V_1 = V_{EN1} + V_{BE1} + I_{B1}R_S = V_{EN} + V_{\gamma 1}$$

If $R_E(h_{FE} + 1) >> R_B$, the drop across R_B may be neglected compared to the drop across R_E.

$$\therefore \quad V_{EN} = V' - V_{BE2}$$

and $$V_1 = V' - V_{BE2} + V_{\gamma 1}$$

Since V_{yJ} is the voltage from base to emitter at cut-in where the loop gain just exceeds unity, it differs from V_{BE2} in the active region by only 0.1 V for either Ge or Si. $V_1 = V' - 0.1$

This indicates that V, may be made almost independent of h^, of the emitter resistance R_E, of the temperature and of whether or not a silicon or germanium transistor is used. Hence the discriminator level V_t is stable with transistor replacement, ageing, temperature changes, provided that (/IPE + l)/?E » R_B and that V" » 0.1. Since V depends on V_{CC}, *RCI*, *R*\ and R_2, where stability is required it is necessary that a stable supply and stable resistors are selected.

Derivation of expression for LTP

The lower triggering point LTP is defined as the input voltage V_2 at which the transistor Q_2 resumes conduction. *Vi* can be calculated from the circuit shown in Figure 4.33 which is obtained by replacing V_{cc}, J?$_{C1}$, *RI* and R_2 of Figure 4.29 by Thevenin's equivalent voltage VTH and Thevenin's equivalent resistance *R* at the collector of $Q_(,$ where

$$V_{Th} = V_{CC}\frac{R_1+R_2}{R_{C1}+R_1+R_2} \quad \text{and} \quad R = R_{C1}\|(R_1+R_2) = \frac{R_{C1}(R_1+R_2)}{R_{C1}+R_1+R_2}$$

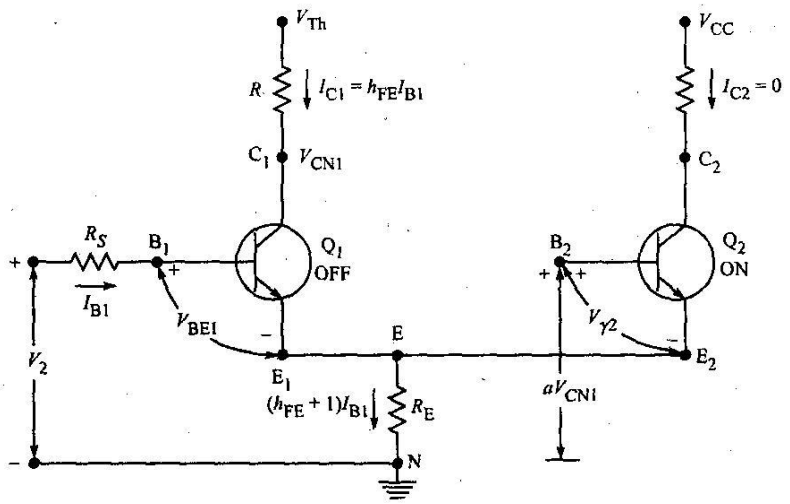


Figure 433 The equivalent circuit of Figure 4.29 when Q_2 just resumes conduction.

The voltage ratio from the collector of Qi to the base of Q_2 is $a = R_2/(R_1 + R_2)$. Figure 4.33, the input signal to Qi is decreasing, and when it reaches V_2 then Q_2 comes out of cut-off.

Writing KVL around the base circuit of Q_2,

$$aV_{CN1} - V_{\gamma 2} - (I_{B1} + I_{C1})R_E = 0$$

where $$V_{CN1} = V_{Th} - I_{C1}R$$

$$\therefore \quad aV_{Th} - aI_{C1}R - V_{\gamma 2} - I_{C1}\left(1+\frac{1}{h_{FE}}\right)R_E = 0$$

or $$I_{C1} = \frac{aV_{Th} - V_{\gamma 2}}{aR + R_E\left(1+\frac{1}{h_{FE}}\right)}$$

$$\therefore \quad aV_{Th} = \frac{R_2}{R_1+R_2} \cdot V_{CC}\frac{R_1+R_2}{R_1+R_2+R_{C1}} = V_{CC}\frac{R_2}{R_2+R_{C1}+R_i} = V'$$

Let $$R_E\left(1+\frac{1}{h_{FE}}\right) = R'_E$$

$$\therefore \quad I_{C1} = \frac{V' - V_{\gamma 2}}{aR + R'_E}$$

Therefore from Figure 4.33,

$$V_2 = I_{B1}R_S + V_{BE1} + (I_{B1} + I_{C1})R_E$$

$$= V_{BE1} + I_{C1}\left(R_E\left(1+\frac{1}{h_{FE}}\right)+\frac{R_S}{h_{FE}}\right)$$

$$= V_{BE1} + I_{C1}\left(R'_E + \frac{R_S}{h_{FE}}\right)$$

$$= V_{BE1} + \frac{V' - V_{\gamma 2}}{aR + R'_E}\left(R'_E + \frac{R_S}{h_{FE}}\right)$$

Since h_{FE} is a large number, $R'_E \approx R_E$ and usually $\frac{R_S}{h_{FE}} << R_E$

$$\therefore \qquad V_2 = V_{BE1} + (V' - V_{\gamma 2})\frac{R_E}{aR + R_E}$$

Since $V_{BE|}$ is higher for silicon than germanium, the LTP Va is a few tenths of a volt higher for a Schmitt trigger using silicon transistors than for one using germanium transistors.

MONOSTABLE MULTIVIBRATOR

As the name indicates, a monostable multivibrator has got only one permanent stable state, the other state being quasi stable. Under quiescent conditions, the monostable multivibrator will be in its stable state only. A triggering signal is required to induce a transition from the stable state to the quasi stable state. Once triggered properly the circuit may remain in its quasi stable state for a time which is very long compared with the time of transition between the states, and after that it will return to its original state. No external triggering signal is required to induce this reverse transition. In a monostable multivibrator one coupling element is a resistor and another coupling element is a capacitor.

When triggered, since the circuit returns to its original state by itself after a time *T*, it is known as a one-shot, a single-step, or a univibrator. Since it generates a rectangular waveform which can be used to gate other circuits, it is also called a *gating circuit.* Furthermore, since it generates a fast transition at a predetermin6d time *T* after the input trigger, it is also referred to as a *delay circuit.* The monostable multivibrator may be a collector-coupled one, or an emitter-coupled one.

THE COLLECTOR COUPLED MONOSTABLE MULTIVIBRATOR

Figure 4.41 shows the circuit diagram of a collector-to-base coupled (simply called collector-coupled) monostable multivibrator using n-p-n transistors. The collector of Q_2 is coupled to the base of Qi by a resistor R_J (dc coupling) and the collector of Q_t is coupled to the base of Q_2 by a capacitor *C* (ac coupling). Ci is the commutating capacitor introduced to increase the speed of operation. The base of Qi is connected to $-V_{BB}$ through a resistor R_2, to ensure that Q! is cut off under quiescent conditions. The

base of Q_2 is connected to V_{CC} through R to ensure that Q_2 is ON under quiescent conditions. In fact, R may be returned to even a small positive voltage but connecting it to V_{cc} is advantageous.

The circuit parameters are selected such that under quiescent conditions, the monostable multivibrator finds itself in its permanent stable state with Q_2ON (i.e. in saturation) and Q! OFF (i.e. in cut-off)- The multivibrator may be induced to make a transition out of its stable state by the application of a negative trigger at the base of Q_2 or at the collector of Q|. Since the triggering signal is applied to only one device and not to both the devices simultaneously, unsymmetrical triggering is employed.

When a negative signal is applied at the base of Q_2 at $t \sim 0$, due to regenerative action Q_2 goes to OFF state and Qi goes to ON state. When Q, is ON, a current /i flows through its R_c and hence its collector voltage drops suddenly by $I\backslash R_C$ This drop will be instantaneously

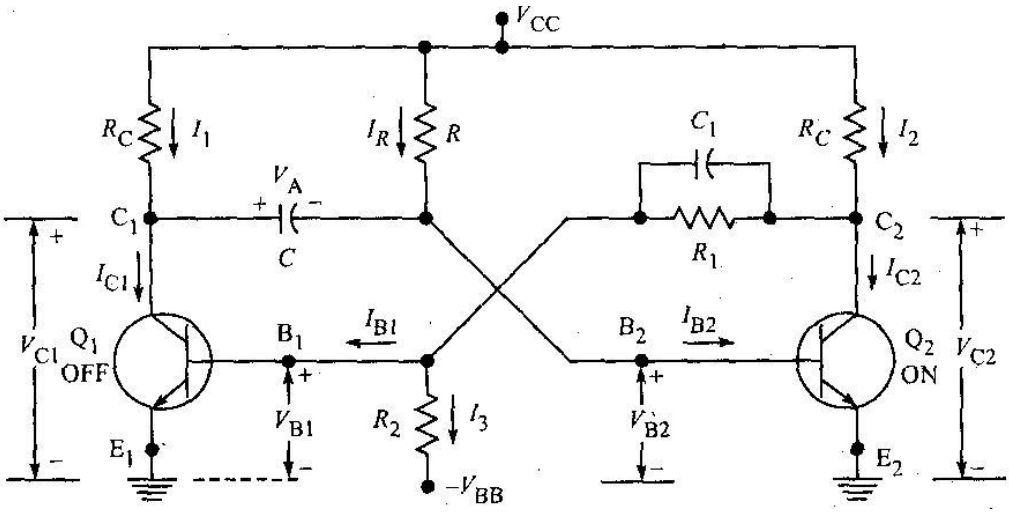


Figure 4.41 Circuit diagram of a collector-coupled monostable multivibrator.

transmitted through the coupling capacitor C to the base of Q_2. So at $t = 0^+$, the base voltage of Q_2 is

$$V_{BE}(\text{sat}) - I_1 R_C.$$

The circuit cannot remain in this state for a long time (it stays in this state only for a finite time *T)* because when Q_t conducts, the coupling capacitor *C* charges from V_{cc} through the conducting transistor Qi and hence the potential at the base of Q_2 rises exponentially with a time constant $(R + R_o)C \approx RC$, where R_0 is the conducting transistor output impedance including the resistance R_c. When it passes the cut-in voltage V_y of Q_2 (at a time $t = T$), a regenerative action takes place turning Q| OFF and eventually returning the multivibrator to its initial stable state.

The transition from the stable state to the quasi-stable state takes place at $t = 0$, and the reverse transition from the quasi-stable state to the stable state takes place at $t = T$. The time T for which the circuit is in its quasi-stable state is also referred to as the delay time, and also as the gate width, pulse width, or pulse duration. The delay time may be varied by varying the time constant $t(= RC)$.

Expression for the gate width T of a monostable multivibrator neglecting the reverse saturation current /CBO

Figure 4.42(a) shows the waveform at the base of transistor Q_2 of the monostable multivibrator shown in Figure 4.41.

For $t < 0$, Q_2 is ON and so $v_{B2} = V_{BE}(sat)$. At $t = 0$, a negative signal applied brings Q_2 to OFF state and Q[into saturation. A current /| flows through R_c of Q_t and hence v_{ci} drops abruptly by /|7? $_c$ volts and so v_{B2} also drops by $I\backslash R_C$ instantaneously. So at t - 0, $v_{B2} = V_{BE}(sat)$ - I_JR_C. For $t > 0$, the capacitor charges with a time constant RC, and hence the base voltage of Q_2 rises exponentially towards V_{CC} with the same time constant. At $t = T$, when this base voltage rises to the cut-in voltage level Vy of the transistor, Q_2 goes to ON state, and Qj to OFF state and the pulse ends.

In the interval $0 < t < 7"$, the base voltage of Q_2, i.e. v_{B2} is given by

$$v_{B2} = V_{CC} - (V_{CC} - \{V_{BE}(sat) - I_1R_C\})e^{-t/\tau}$$

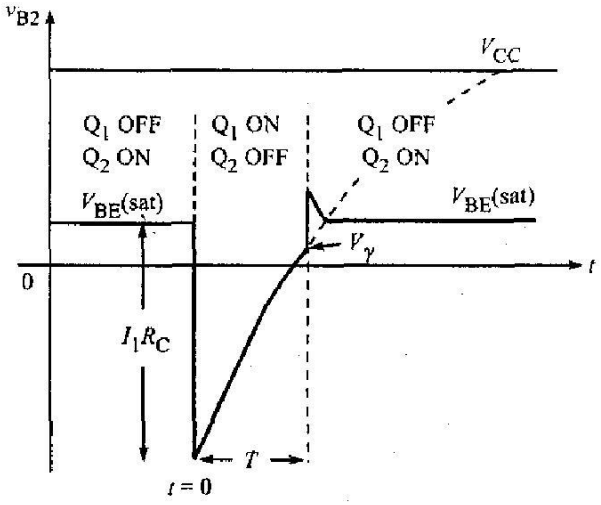


Figure 4.42(a) Voltage variation at the base of Q_2 during the quasi-stable state (neglecting /cuoX

But $I_1R_C = V_{CC} - V_{CE}(\text{sat})$ (because at $t = 0^-$, $v_{C1} = V_{CC}$ and at $t = 0^+$, $v_{C1} = V_{CE}(\text{sat})$)

$$\therefore \quad v_{B2} = V_{CC} - [V_{CC} - \{V_{BE}(\text{sat}) - (V_{CC} - V_{CE}(\text{sat}))\}]e^{-t/\tau}$$

$$= V_{CC} - [2V_{CC} - \{V_{BE}(\text{sat}) + V_{CE}(\text{sat})\}]e^{-t/\tau}$$

At $t = T$, $v_{B2} = V_\gamma$

$$\therefore \quad V_\gamma = V_{CC} - [2V_{CC} - \{V_{CE}(\text{sat}) + V_{BE}(\text{sat})\}]e^{-T/\tau}$$

i.e.
$$e^{T/\tau} = \frac{2V_{CC} - [V_{CE}(\text{sat}) + V_{BE}(\text{sat})]}{V_{CC} - V_\gamma}$$

$$\therefore \quad \frac{T}{\tau} = \frac{\ln\left[2\left(V_{CC} - \frac{V_{CE}(\text{sat}) + V_{BE}(\text{sat})}{2}\right)\right]}{V_{CC} - V_\gamma}$$

i.e.
$$T = \tau \ln 2 + \tau \ln \frac{V_{CC} - \frac{V_{CE}(\text{sat}) + V_{BE}(\text{sat})}{2}}{V_{CC} - V_\gamma}$$

Normally for a transistor, at room temperature, the cut-in voltage is the average of the saturation junction voltages for either Ge or Si transistors, i.e. $V_\gamma = \frac{V_{CE}(\text{sat}) + V_{BE}(\text{sat})}{2}$

Neglecting the second term in the expression for T

$$T = \tau \ln 2$$

i.e.
$$T = (R + R_a)C \ln 2 = 0.693(R + R_a)C$$

but for a transistor in saturation $R_a \ll R$.

Gate width, $T = 0.693KC$

The larger the V_{cc} is, compared to the saturation junction voltages, the more accura the result is.

The gate width can be made very stable (almost independent of transistor characteristic supply voltages, and resistance values) if Q_l is driven into saturation during the quasi-stab state.

Expression for the gate width of a monostable multivibrator considering th reverse saturation current /CBO

In the derivation of the expression for gate width T above, we neglected the effect of tt reverse saturation current /CBO on the gate width T. In fact, as the temperature increases, tt reverse saturation current increases and the gate width decreases.

In the quasi-stable state when Q_2 is OFF, /CBO flows out of its base through R to th supply V_{cc}. Hence the base of Q_2 will be not at V_{cc} but at V_{cc} + /CBO^> ^ C *S disconnect from the junction of the base of Q_2 with the resistor R. It therefore appears that the capacitt C in effect charges through R from a source V_{cc} + /CBO^- See Figure 4.42(b).

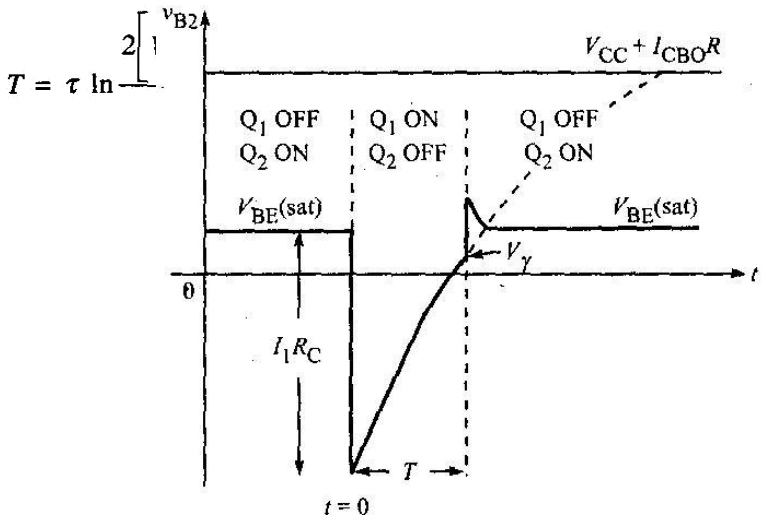


Figure 4.42(b) Voltage variation at the base of Q_2 during the quasirstable state (considering

So, the expression for the voltage at the base of Q_2 is given by

$$v_{B2} = (V_{CC} + I_{CBO}R) - [(V_{CC} + I_{CBO}R) - (V_{BE}(sat) - I_1R_C)]e^{-t/\tau}$$

$$= (V_{CC} + I_{CBO}R) - [(V_{CC} + I_{CBO}R) - (V_{BE}(sat) - (V_{CC} - V_{CE}(sat))]e^{-t/\tau}$$

At $t = T$, $v_{B2} = V_\gamma$

$$\therefore \quad V_\gamma = V_{CC} + I_{CBO}R - [2V_{CC} + I_{CBO}R - (V_{CE}(sat) + V_{BE}(sat))]e^{-T/\tau}$$

$$\therefore \quad e^{T/\tau} = \frac{2V_{CC} + I_{CBO}R - (V_{CE}(sat) + V_{BE}(sat))}{V_{CC} + I_{CBO}R - V_\gamma}$$

Neglecting the junction voltages and the cut-in voltage of the transistor,

$$T = \tau \ln \frac{2\left[V_{CC} + \frac{I_{CBO}R}{2}\right]}{V_{CC} + I_{CBO}R}$$

$$= \tau \ln 2 + \tau \ln \frac{1 + \frac{\phi}{2}}{1 + \phi}, \quad \text{where } \phi = \frac{I_{CBO}R}{V_{CC}}$$

$$T = \tau \ln 2 - \tau \ln \frac{1 + \phi}{1 + \frac{\phi}{2}}$$

Since $/_{CBO}$ increases with temperature, we can conclude that the delay time T decreases as temperature increases.

Waveforms of the collector-coupled monostable multivibrator

The waveforms at the collectors and bases of both the transistors Q] and Q_2 of the monostable multivibrator of Figure 4.41 are shown in Figure 4.44.

The triggering signal is applied at $t = 0$, and the reverse transition occurs at $t = T$.

The stable state. For $t < 0$, the monostable circuit is in its stable state with Q_2 ON and Q, OFF. Since Q_2 is ON, the^ase voltage of Q_2 is $v_{B2} = V_{BE2}(sat)$ and the collector voltage of Q_2 is $v_{C2} = V_{CE2}(sat)$. Since Q, is OFF, there is no current in R_C of Q! and its base voltage must be negative. Hence the voltage at the collector of Q| is, $v_{C1} = V_{CC}$

and the voltage at the base of Q] using the superposition theorem is

$$v_{B1} = -V_{BB}\frac{R_1}{R_1 + R_2} + V_{CE2}(sat)\frac{R_2}{R_1 + R_2}$$

***The quasi-stable** state.* A negative triggering signal applied at $t = 0$ brings Q_2 to OFF state and Qi to ON state. A current /, flows in tf_c of Q]. So, the collector voltage of Qj drops suddenly by I_jR_C volts. Since the voltage across the coupling capacitor C cannot change instantaneously, the voltage at the base of Q_2 also drops by $/itf_c$, where $I_{\{}R_C = V_{cc}$ -VcE2(^{sat})- Since Qi is ON,

$$v_{B1} = V_{BE1}(sat) \quad \text{and} \quad v_{C1} = V_{CE1}(sat)$$

$$\text{Also,} \quad v_{B2} = V_{BE2}(sat) - I_1R_C \quad \text{and} \quad v_{C2} = V_{CC}\frac{R_1}{R_1 + R_C} + V_{BE1}(sat)\frac{R_C}{R_1 + R_C}$$

In the interval $0 < t < T$, the voltages VGI, VBI and Vc2 remain constant at their values at f = 0, but the voltage at the base of. Q_2, i.e. v_{B2} rises exponentially towards V_{cc} with a time constant, t - RC, until at $t = T$, v_B2 reaches the cut-in voltage V_x of the transistor.

Waveforms for $t > T$. At / = 7*[1]", reverse transition -takes place. Q_2 conducts and Qi is cut-off. The collector voltage of Q_2 and the base voltage of Qi return to their voltage levels for / < 0. The voltage v_{cl} now rises abruptly since Q_t is OFF. This increase in voltage is transmitted to the base of Q_2 and drives Q_2 heavily into saturation. Hence an overshoot develops in v_{B2} at t = 7**", which decays as the capacitor recharges because of the base current. The magnitude of the base current may be calculated as follows. Replace the input circuit of Q_2 by the base spreading resistance r_{BB} in series with the voltage VsE(sat) as shown in Figure 4.43. Let 7_B be the base current at $t = 1$*. The current in R may be neglected compared to $/'_B$.

From Figure 4.43,

$$V'_{BE} = I'_B r'_{BB} + V_{BE}(\text{sat}) \quad \text{and} \quad V_C = V_{CC} - I'_B R_C - V'_{BE}$$

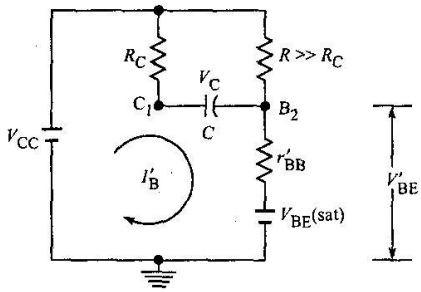


Figure 4.43 Equivalent circuit for calculating the overshoot at base 62 of Q_3.

The jumps in voltages at B_2 and C| are, respectively, given by

$$\delta = V'_{BE} - V_\gamma = I'_B r'_{BB} + V_{BE}(\text{sat}) - V_\gamma \quad \text{and} \quad \delta' = V_{CC} - V_{CE}(\text{sat}) - I'_B R_C$$

Since C] and B_2 are connected by a capacitor C and since the voltage across the capacitts cannot change instantaneously, these two discontinuous voltage changes 5 and 5' must bl equal.

Equating them,

$$I'_B r'_{BB} + V_{BE}(\text{sat}) - V_\gamma = V_{CC} - V_{CE}(\text{sat}) - I'_B R_C$$

$$I'_B = \frac{V_{CC} - V_{BE}(\text{sat}) - V_{CE}(\text{sat}) + V_\gamma}{R_C + r'_{BB}}$$

v_{B2} and v_{cl} decay to their steady-state values with a time constant $\tau' = (R_C + r'_{BB})C$

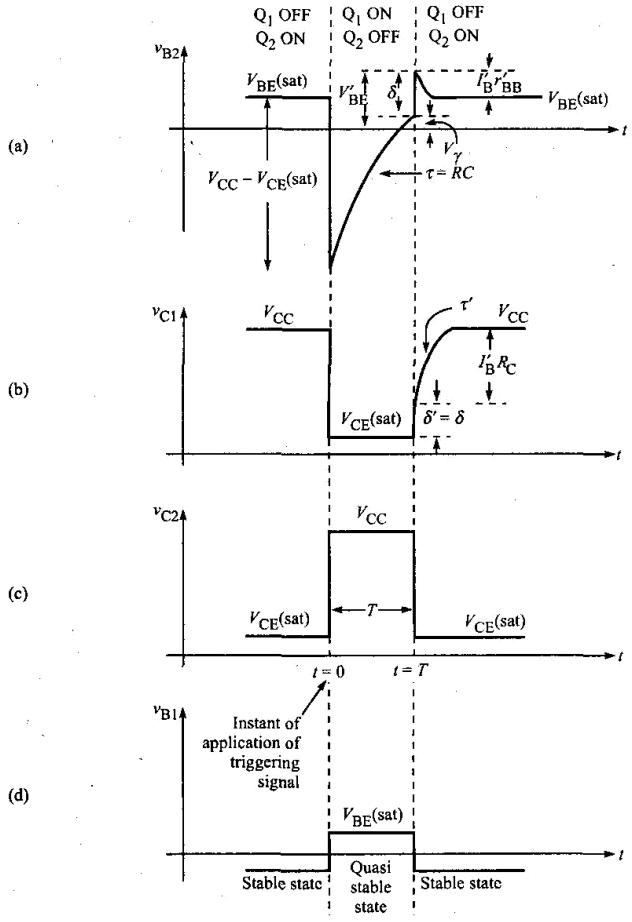


Figure 4.44 Waveforms at the collectors and bases of the collector-coupled monostable multivibrator. (a) at the base of Q_2, (b) at the collector of Q_t, (c) at the collector of Q_2, and (d) at the base o

ASTABLE MULTIVIBRATOR

As the name indicates an astable multivibrator is a multivibrator with no permanent stable state. Both of its states are quasi stable only. It cannot remain in any one of its states indefinitely and keeps on oscillating between its two quasi stable states the moment it is connected to the supply. It remains in each of its two quasi stable states for only a short designed interval of time and then goes to the other quasi stable state. No triggering signal is required. Both the coupling elements are capacitors (ac coupling) and hence both the states are quasi stable. It is a free running multivibrator. It generates square waves. It is used as a master oscillator.

There are two types of astable multivibrators:

1. Collector-coupled astable multivibrator
2. Emitter-coupled astable multivibrator

THE COLLECTOR-COUPLED ASTABLE MULTIVIBRATOR

Figure 4.53 shows the circuit diagram of a collector-coupled astable multivibrator using n-p-n transistors. The collectors of both the transistors Qj and Q_2 are connected to the bases

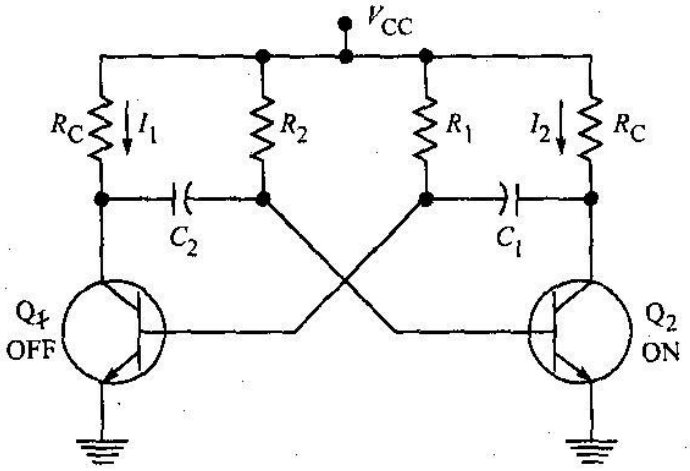


Figure 4.53 A collector-coupled astable multivibrator.

of the other transistors through the coupling capacitors C_s and C_2. Since both are ac couplings, neither transistor can remain permanently at cut-off. Instead, the circuit has two quasi-stable states, and it makes periodic transitions between these states. Hence it is used as a master oscillator. No triggering signal is required for this multivibrator. The component values are selected such that, the moment it is connected to the supply, due to supply transients one transistor will go into saturation and the other into cut-off, and also due to capacitive couplings it keeps on-oscillating between its two quasi stable states.

The waveforms at the bases and collectors for the astable multivibrator, are shown in Figure 4.54. Let us say at $t = 0$, Q_2 goes to ON state and Q] to OFF state. So, for $t < 0$, Q_2 was OFF and Qi was ON. Hence

for $t < 0$, v_{B2} is negative, $v_{C2} = V_{cc}$, $v_{B!} = V_{BE}(sat)$ and $v_{cj} = V_{CE}(sat)$. The capacitor C_2 charges from V_{cc} through R_2 and v_{B2} rises exponentially towards V_{cc}. At $t = 0$, v_{B2} reaches the cut-in voltage V_y and Q_2 conducts. As Q_2 conducts, its collector voltage Vc_2 drops by /2/?c - ^cc ~ VcE(^{sa}O- This drop in vc_2 is transmitted to the base of Qj through the coupling capacitor C_2 and hence v_{B1} also falls by /2/?c- Qi goes to OFF state. So, $v_{B]} = V_{BE}(sat) - /_2tf_c$, and its collector voltage v_{cl} rises towards V_{CC}- This rise in $v_{c]}$ is coupled through the coupling capacitor C_2 to the base of Q_2, causing an overshoot *§* in v_{B2} and the abrupt rise by the same amount *8* in VCL as shown in Figure 4.51(c). Now since Q_2 is ON, *C* charges from V_{cc} through R_{lt} and hence $v_{B]}$ rises exponentially. At t = 7"], when $v_{B!}$ rises to V_Y, Qi conducts and due to regenerative action Qi goes into saturation and Q_2 to cut-off. Now, for $t > T$\, the coupling capacitor C_2 charges from V_{cc} through R_2 and at / = 7", + 7"2, when v_{B2} rises to the cut-in voltage V_r, Q_2 conducts and due to regenerative feedback Q_2 goes to ON state and Q| to OFF state. The cycle of events repeats and the circuit keeps on oscillating between its two quasi-stable states. Hence the output is a square wave. It is called a square wave generator or square wave oscillator or relaxation oscillator. It is a free running oscillator.

Expression for the frequency of oscillation of an astable multivibrator

Consider the waveform at the base of Q_1 shown in Figure 4.54(d). At $t = 0$,

$$v_{B1} = V_{BE}(sat) - I_2R_C$$

But
$$I_2R_C = V_{CC} - V_{CE}(sat)$$

$\therefore$ At $t = 0$, $v_{B1} = V_{BE}(sat) - V_{CC} + V_{CE}(sat)$

For $0 < t < T_1$, v_{B1} rises exponentially towards V_{CC} given by the equation,

$$v_o = v_f - (v_f - v_i)e^{-t/\tau}$$

$\therefore$ $v_{B1} = V_{CC} - [V_{CC} - (V_{BE}(sat) - V_{CC} + V_{CE}(sat))]e^{-t/\tau_1}$, where $\tau_1 = R_1C_1$

At $t = T_1$, when v_{B1} rises to V_γ, Q_1 conducts

$\therefore$
$$V_\gamma = V_{CC} - [2V_{CC} - (V_{BE}(sat) + V_{CE}(sat))]e^{-T_1/R_1C_1}$$

or
$$e^{T_1/R_1C_1} = \frac{2\left[V_{CC} - \frac{V_{BE}(sat) + V_{CE}(sat)}{2}\right]}{V_{CC} - V_\gamma}$$

$$T_1 = R_1C_1 \ln \frac{2\left[V_{CC} - \frac{V_{CE}(sat) + V_{BE}(sat)}{2}\right]}{V_{CC} - V_\gamma}$$

$$T_1 = R_1C_1 \ln 2 + R_1C_1 \ln \frac{\left[V_{CC} - \frac{V_{CE}(sat) + V_{BE}(sat)}{2}\right]}{V_{CC} - V_\gamma}$$

At room temperature for a transistor,

$$V_\gamma \simeq \frac{V_{CE}(sat) + V_{BE}(sat)}{2}$$

$\therefore$
$$T_1 = R_1C_1 \ln 2 = 0.693R_1C_1$$

On similar lines considering the waveform of Figure 4.54(b), we can show that the time T_2 for which Q_2 is OFF and Qj is ON is given by $T_2 = R_2C_2 \ln 2 = 0.693R_2C_2$ The period of the waveform, The frequency of oscillation,

If $R_f = R_2 = R$, and $C_s = C_2 = C$, then TI = T_2 = 772

$$T = 2 \times 0.693RC = 1.386RC \qquad \text{and} \qquad f = \frac{\text{I}}{1.386RC}$$

The frequency of oscillation may be varied over the range from cycles to mega cycles by varying *RC*. It is also possible to vary the frequency electrically by connecting *R*\ and R_2 to an auxiliary voltage source *V* (the collector supply remains $+V_{CC}$) and then varying this voltage *V*.

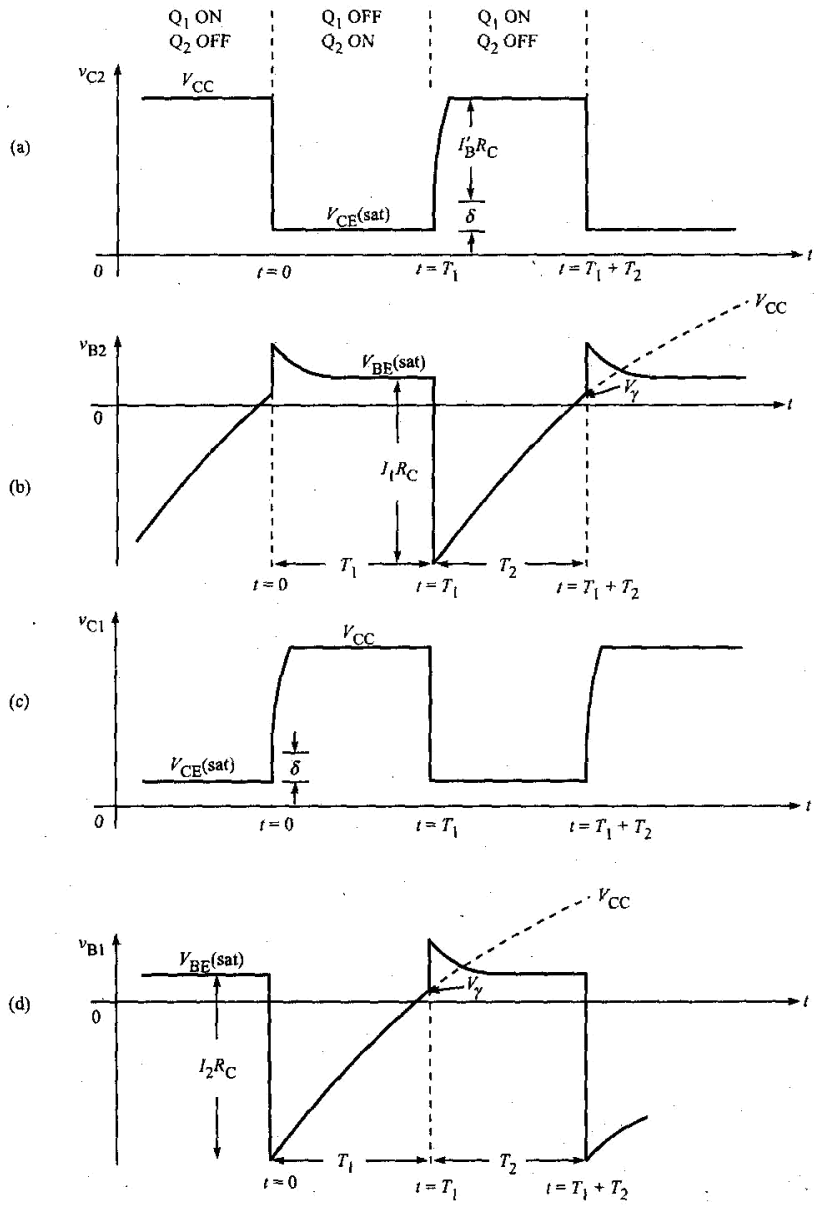


Figure 4.54 Waveforms at the bases and collectors of a collector-coupled astable multivibrator.

THE EMITTER-COUPLED ASTABLE MULTIVIBRATOR

An emitter-coupled astable multivibrator may be obtained by using three power supplies or a single power supply.

Figure 4.63 shows the circuit diagram of a free-running emitter coupled multivibrator using n-p-n transistors. Figure 4.64 shows its waveforms. Three power supplies are indicated for the sake of simplifying the analysis. A more practical circuit using a single supply is indicated in Figure 4.65. Let us assume that the circuit operates in such a manner that Qi switches between cut-off and saturation and Q_2 switches between cut-off and its active region.

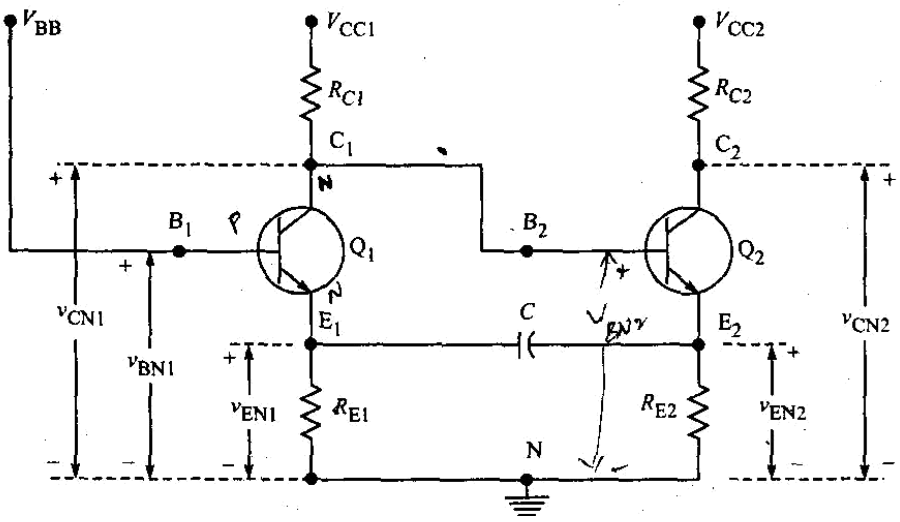


Figure 4.63 The astable emitter-coupled multivibrator.

Calculations at $t = t_1^-$

Since Q_1 is ON and Q_2 is OFF just before the transition at $t = t_1^-$, we have

$$v_{CN2}(t_1^-) = V_{CC2}$$
$$v_{EN1}(t_1^-) = V_{BB} - V_{BE}(\text{sat}) = V_{BB} - V_\sigma$$
$$v_{CN1}((t_1^-) = v_{BN2} = v_{EN1} + V_{CE}(\text{sat}) = V_{BB} - V_\sigma + V_{CE}(\text{sat})$$

During the interval preceding $t = t$\, the capacitor C charges from a fixed voltage ^BB ~ *V0* through the resistor R_{E2}. All circuit voltages remain constant except v_{EN2}, which falls asymptotically towards zero.

The transistor Q_2 will begin to conduct when v_{EN2} falls to $v_{EN2}(t_1^-) = v_{BN2} - V_\sigma + V_{CE}(\text{sat}) - V_\gamma$

Calculations at f = tf

When Q_2 conducts, v_{EN2} and v_{EN1} rise. As v_{EN}i rises, Q] comes out of saturation and v_{CN1} (= v_{BN2}) also increases, causing a further increase in the current in Q_2. Because of this regenerative action, Qi is driven OFF and Q_2 is driven into its active region where its base-to-emitter voltage is V_{BE2}, its base current is $/_{B2}$ and its collector current is $/_{C2}$. From Figure 4.64, we see that after transition, at t = rf.

$$v_{CN2}(t_1^+) = V_{CC2} - I_{C2}R_{C2}$$
$$v_{CN1}(t_1^+) = v_{BN2}(t_1^+) = V_{CC1} - I_{B2}R_{C1}$$
$$v_{EN2}(t_1^+) = v_{BN2}(t_1^+) - v_{BE2}(t_1^+) = V_{CC1} - I_{B2}R_{C1} - v_{BE2}$$

At t\ there is an abrupt change V_p in v_{EN2}.

Because of the capacitive coupling between emitters there must also be the same discontinuity VD in VENI. Hence,

$$V_D = v_{EN1}(t_1^+) - v_{EN1}(t_1^-) = v_{EN2}(t_1^+) - v_{EN2}(t_1^-)$$

i.e.
$$v_{EN}(t_1^+) = V_{CC1} - I_{B2}R_{C1} - V_{BE2} - V_{CE}(\text{sat}) + V_\gamma = V_1$$

Neglecting junction voltages and /$_{B2}$^ci compared with V_{CC}i $v_{EN1}(t_1^+) = v_{EN2}(t_1^+) \simeq V_{CC1}$

The period

The interval T\ when Q_2 conducts and Qi is OFF ends at $t = t_2$- The transistor Q_t will turn ON when the base-to-emitter voltage reaches the cut-in value V_y or when V_{EN}i reaches the voltage

$$v_{EN1}(t_2^-) = V_{BB} - V_\gamma$$

Since the base voltage of Qi is fixed, then to carry the transistor from the cut-in point to saturation the emitter must drop. However this drop S is small, since $S = V_a \sim V_r = 0.2$ V. Because the emitters are capacitively coupled there will be an identical jump S *in* v_EN_2, After / = t_2, in the interval T_2, conditions are the same as they were for $t < t$\.

Therefore, the cycle of events described above is repeated and the circuit behaves as an astable multivibrator.

From Figure 4.64(a), we see that the voltage v_{ENI} starts at V\ at $t = t$\ and falls to *^BB - Vj,at f = t_2. Since this decay is exponential with a time constant #E|C and approaches zero asymptotically, $v_{EN1} = 0 - (0 - V_1)e^{-t/\tau}$

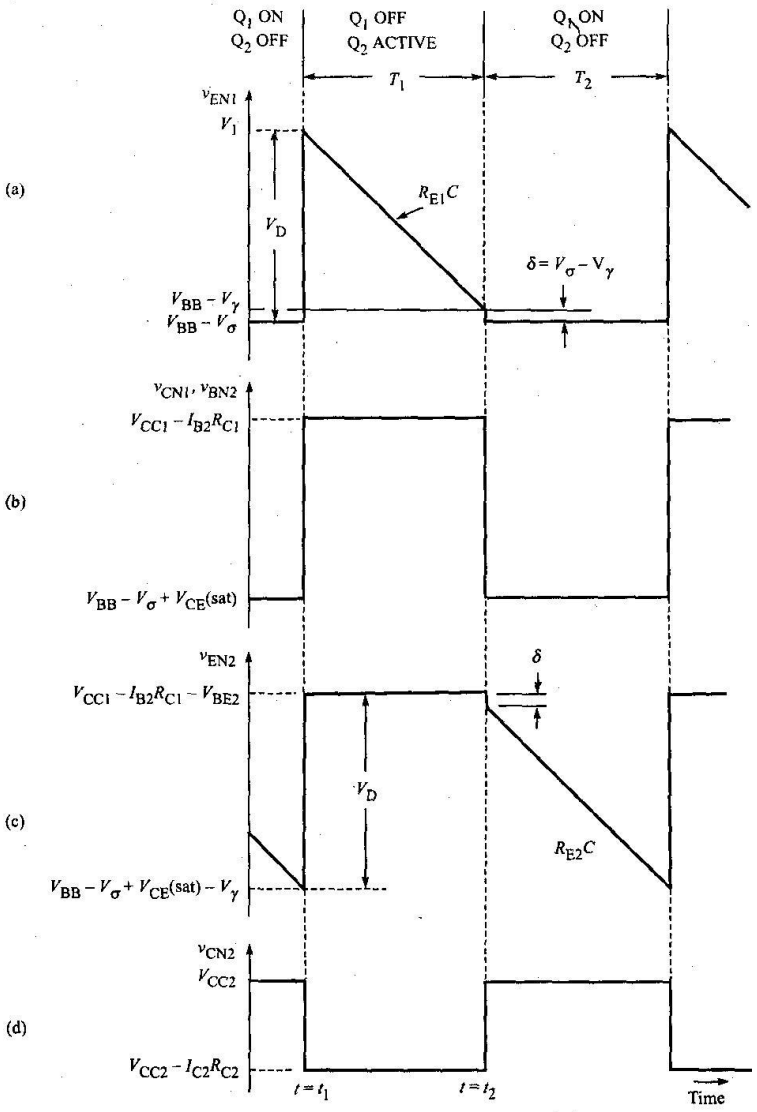


Figure 4.64 Waveforms of the emitter-coupled astable multivibrator.

At $t = T_1,\ v_{EN1} = V_{BB} - V_\gamma$

$$\therefore \quad V_{BB} - V_\gamma = V_1 e^{-T_1/\tau}$$

$$\therefore \quad T_1 = \tau \ln \frac{V_1}{V_{BB} - V_\gamma}$$

i.e.

$$T_1 = R_{E1} C \ln \frac{V_1}{V_{BB} - V_\gamma}$$

Assuming that the supply voltages are large compared with the junction voltages and assuming also that

$$T_1 = R_{E1} C \ln \frac{V_{CC1}}{V_{BB}}$$

/B2^Ei « ^ccb we find

Subject to the same approximations, T_2 is given by

$$T_2 = R_{E2} C \ln \frac{V_{CC1}}{V_{BB}}$$

If V_{CC}| and V_{BB} are arranged to be proportional to one another, then the frequency is independent of the supply voltages.

When QJ is OFF, its collector-to-ground voltage is approximately V_{CC1} and equals the base-to-ground voltage of Q_2. Since it is desired that Q_2 be in its active region, then V_{BN2} should be less than V_{CN2} or $V_{CC[}$ < V_{CC2}. Since Qj is to be driven into saturation, then its base voltage may be almost as large as its collector supply voltage. However, to avoid driving *Q*\ too deeply into saturation it is better to arrange that V_{BB} < V_{CC1}, A circuit which uses a single supply and which satisfies the requirements that V_{BB} be proportional to V_{ca} and that V_{BB} < V_{CC1} < V_{CC2} is shown in Figure 4.65. Since *C'* is a bypass capacitor intended to maintain V_{BB} constant, it is not involved in the operation of the circuit. We assume that /?! and *RI* are small enough so that the voltage V_{BB} at the junction of *RJ* and *R2* remains normally constant during the entire cycle of operations of the multivibrator. Using Thevenin's theorem we see that the circuit of Figure 4.65 is of the same form as that of Figure 4.63 with V_{CC2} ~ ^cc [a]°d with

$$R_{C1} = \frac{R'R''}{R'+R''}$$

and

$$V_{CC1} = V_{CC}\frac{R''}{R'+R''} + V_{BB}\frac{R'}{R'+R''}$$

The advantages and disadvantages of the emitter-coupled astable multivibrator over the collector-coupled astable multivibrator are given below:

Advantages

1. It is inherently self-starting.
2. The collector of Q_2 where the output is taken may be loaded heavily even capacitively.
3. The output is free of recovery transients.
4. Because it has an isolated input at the base of Qi, synchronization is convenient.
5. Frequency adjustment is convenient because only one capacitor is used.

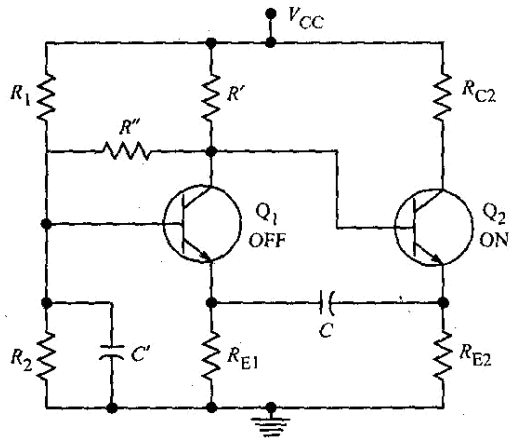


Figure 4.65 The emitter-coupled multivibrator.

Disadvantages

1. This circuit is more difficult to adjust for proper operating conditions.
2. This circuit cannot be operated with T\ and T_2 widely different.
3. This circuit uses more components than does the collector-coupled circuit.

UNIT – IV
TIME BASE GENERATORS

TIME BASE GENERATORS

A time-base generator is an electronic circuit which generates an output voltage or current waveform, a portion of which varies linearly with time. Ideally the output waveform should be a ramp. Time-base generators may be voltage time-base generators or current time-base generators. A voltage time-base generator is one that provides an output voltage waveform, a portion of which exhibits a linear variation with respect to time. A current time-base generator is one that provides an output current waveform, a portion of which exhibits a linear variation with respect to time. There are many important applications of time-base generators, such as in CROs, television and radar displays, in precise time measurements, and in time modulation. The most important application of a time-base generator is in CROs. To display the variation with respect to time of an arbitrary waveform on the screen of an oscilloscope it is required to apply to one set of deflecting plates a voltage which varies linearly with time. Since this waveform is used to sweep the electron beam horizontally across the screen it is called the *sweep voltage* and the time-base generators are called the *sweep* circuits.

GENERAL FEATURES OF A TIME-BASE SIGNAL

Figure 5.1(a) shows the typical waveform of a time-base voltage. As seen the voltage starting from some initial value increases linearly with time to a maximum value after which it returns again to its initial value. The time during which the output increases is called the *sweep time* and the time taken by the signal to return to its initial value is called the *restoration time,* the *return time,* or *the flyback time.* In most cases the shape of the waveform during restoration time and the restoration time itself are not of much consequence. However, in some cases a restoration time which is very small compared with the sweep time is required. If the restoration time is almost zero and the next linear voltage is initiated the moment the present one is terminated then a saw-tooth waveform shown in Figure 5.1(b) is generated. The waveforms of the type shown in Figures 5.1 (a) and (b) are generally called sweep waveforms even when they are used in applications not involving the deflection of an electron beam.

In fact, precisely linear sweep signals are difficult to generate by time-base generators and moreover nominally linear sweep signals may be distorted when transmitted through a coupling network.

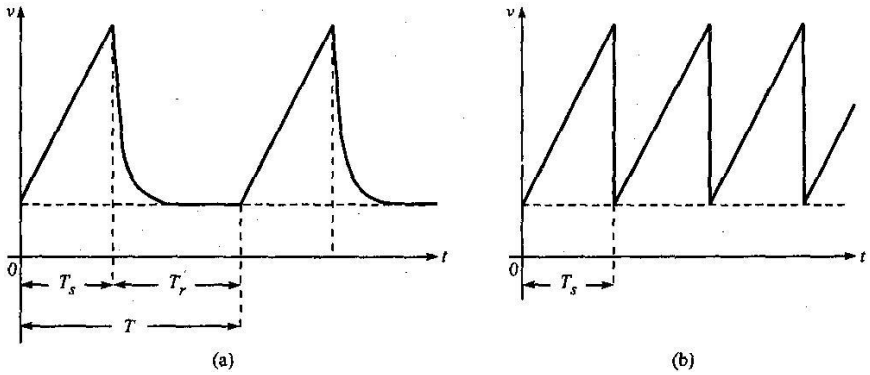


Figure 5.1 (a) General sweep voltage and (b) saw-tooth voltage waveforms.

The deviation from linearity is expressed in three most important ways:

1 . The slope or sweep speed error, e_S

2. The displacement error, e_d

3. The transmission error, e,

The slope or sweep-speed error, e_S

An important requirement of a sweep is that it must increase linearly with time, i.e. the rate of change of sweep voltage with time be constant. This deviation from linearity is defined as

$$\text{Slope or sweep-speed error, } e_s = \frac{\text{difference in slope at beginning and end of sweep}}{\text{initial value of slope}}$$

$$= \frac{\left.\frac{dv_0}{dt}\right|_{t=0} - \left.\frac{dv_0}{dt}\right|_{t=T_s}}{\left.\frac{dv_0}{dt}\right|_{t=0}}$$

The displacement error, e_d

Another important criterion of linearity is the maximum difference between the actual sweep voltage and the linear sweep which passes through the beginning and end points of the actual sweep.

The displacement error e_d is defined as

$$e_d = \frac{\text{maximum difference between the actual sweep voltage and the linear sweep which passes through the beginning and end points of the actual sweep}}{\text{amplitude of the sweep at the end of the sweep time}}$$

$$= \frac{(v_s - v_s')_{\max}}{V_s}$$

As shown in Figure 5.2(a), v_S is the actual sweep and v'_S is the linear sweep.

The transmission error, e_t

When a ramp signal is transmitted through a high-pass circuit, the output falls away from the input as shown in Figure 5.2(b). This deviation is expressed as transmission error e_t, defined as the difference between the input and the output divided by the input at the end of the sweep

$$e_t = \frac{V_s' - V_s}{V_s'}$$

where as shown in Figure 5.2(b), V'_S is the input and V_S is the output at the end of the sweep,

i.e. at $t = T_S$

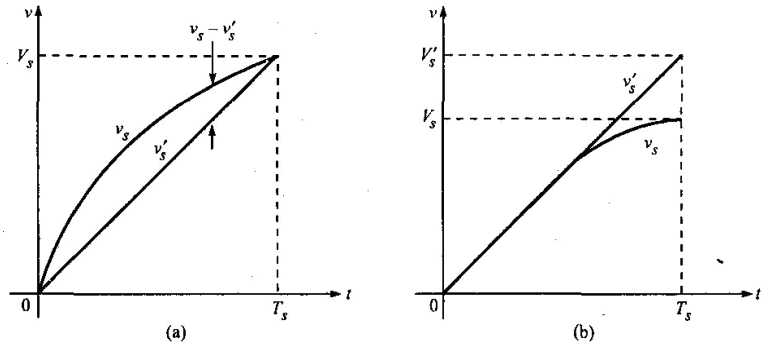


Figure 5.2 (a) Sweep for displacement error and (b) sweep for transmission error.

If the deviation from linearity is small so that the sweep voltage may be approximated by the sum of linear and quadratic terms in *t*, then the above three errors are related as

$$e_d = \frac{e_s}{8} = \frac{e_t}{4}$$

$$e_s = 2e_t = 8e_d$$

which implies that the sweep speed error is the more dominant one and the displacement error is the least severe one.

METHODS OF GENERATING A TIME-BASE WAVEFORM

In time-base circuits, sweep linearity is achieved by one of the following methods.

1. *Exponential charging.* In this method a capacitor is charged from a supply voltage through a resistor to a voltage which is small compared with the supply voltage.
2. *Constant current charging.* In this method a capacitor is charged linearly from a constant current source. Since the charging current is constant the voltage across the capacitor increases linearly.
3. *The Miller circuit.* In this method an operational integrator is used to convert an input step voltage into a ramp waveform.
4. *The Phantastron circuit.* In this method a pulse input is converted into a ramp. This is a version of the Miller circuit.
5. *The bootstrap circuit.* In this method a capacitor is charged linearly by a constant current which is obtained by maintaining a constant voltage across a fixed resistor in series with the capacitor.
6. *Compensating networks.* In this method a compensating circuit is introduced to improve the linearity of the basic Miller and bootstrap time-base generators.
7. *An inductor circuit.* In this method an *RLC* series circuit is used. Since an inductor does not allow the current passing through it to change instantaneously, the current through the capacitor more or less remains constant and hence a more linear sweep is obtained.

EXPONENTIAL SWEEP CIRCUIT

Figure 5.3(a) shows an exponential sweep circuit. The switch S is normally closed and is open at $t = 0$. So for $t > 0$, the capacitor charges towards the supply voltage V with a time constant RC. The voltage across

the capacitor at any instant of time is given by $v_o(t) = V(1 - e^{-t/RC})$ After an interval of time T_x when the sweep amplitude attains the value V_S, the switch again closes. The resultant sweep waveform is shown in Figure 5.3(b).

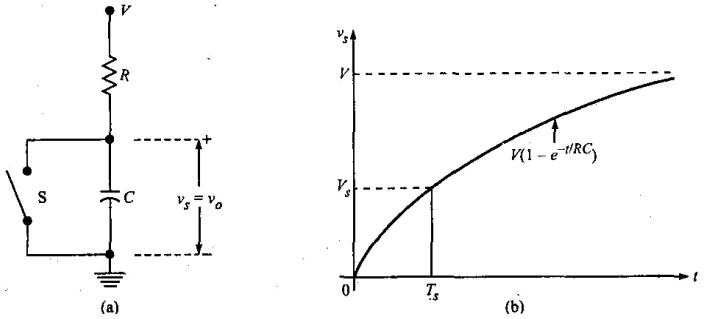


Figure 5.3 (a) Charging a capacitor through a resistor from a fixed voltage and (b) the resultant exponential waveform across the capacitor.

The relation between the three measures of linearity, namely the slope or sweep speed error e_S, the displacement error e_d, and the transmission error e, for an exponential sweep circuit is derived below.

Slope or sweep **speed** error, e_S

We know that for an exponential sweep circuit of Figure 5.3(a),

$$v_o(t) = V(1 - e^{-t/RC})$$

Rate of change of output or slope is

$$\frac{dv_o}{dt} = 0 - V(e^{-t/RC})\left(\frac{-1}{RC}\right) = \frac{Ve^{-t/RC}}{RC}$$

$$\therefore \quad \text{Slope error, } e_s = \frac{\left.\frac{dv_o}{dt}\right|_{t=0} - \left.\frac{dv_o}{dt}\right|_{t=T_s}}{\left.\frac{dv_o}{dt}\right|_{t=0}} = \frac{\frac{V}{RC} - \frac{Ve^{-T_s/RC}}{RC}}{\frac{V}{RC}}$$

$$= 1 - e^{-T_s/RC}$$

$$= 1 - \left(1 - \frac{T_s}{RC} + \left(\frac{-T_s}{RC}\right)^2 \frac{1}{2} + \ldots\right)$$

For small T_S, neglecting the second and higher order terms

$$e_s = \frac{T_s}{RC}$$

Also, $v_o = V(1 - e^{-t/RC})$

At $t = T_s, \quad v_o = V_s$

$$\therefore \quad V_s = V(1 - e^{-T_s/RC}) = V\left[1 - \left(1 - \frac{T_s}{RC} + \left(-\frac{T_s}{RC}\right)^2 \frac{1}{2!} + \ldots\right)\right]$$

Neglecting the second and higher order terms

$$V_s = V\frac{T_s}{RC} \quad \text{or} \quad \frac{V_s}{V} = \frac{T_s}{RC}$$

Hence $$\frac{V_s}{V} = \frac{T_s}{RC} = e_s$$

So the smaller the sweep amplitude compared to the sweep voltage, the smaller will be the slope error.

The transmission error, e,

From Figure 5.2(b),

$$v_s = V(1 - e^{-t/RC})$$

At $t = T_s$,

$$v_s = V_s = V(1 - e^{-T_s/RC})$$

$$= V\left[1 - \left(1 - \frac{T_s}{RC} + \left(-\frac{T_s}{RC}\right)^2 \frac{1}{2!} + \ldots\right)\right]$$

$$V_s = V\left(\frac{T_s}{RC} - \frac{1}{2}\left(\frac{T_s}{RC}\right)^2\right)$$

The initial slope, $\left.\frac{dv_o}{dt}\right|_{t=0} = \frac{V}{RC}$

If the initial slope is maintained at $t = T_s$, $v_s = V_s' = T_s \times \frac{V}{RC}$

$$e_t = \frac{V_s' - V_s}{V_s'} = \frac{\frac{VT_s}{RC} - \left(\frac{VT_s}{RC} - \frac{V}{2}\left(\frac{T_s}{RC}\right)^2\right)}{\frac{VT_s}{RC}} = \frac{T_s}{2RC} = \frac{e_s}{2}$$

The displacement error, e_d

From Figure 5.2(a), we can see that the maximum displacement between the actual sweep and the linear sweep which passes through the beginning and end points of the actual sweep occurs at $t = T_S / 2$

At $t = \frac{T_s}{2}$, $v_s' = \frac{V_s}{2}$ The actual sweep v_S is given by

$$v_s = V(1 - e^{-t/RC})$$

At $t = \frac{T_s}{2}$ $$v_s = V(1 - e^{-T_s/2RC})$$

$$= V\left[1 - \left\{1 - \frac{T_s}{2RC} + \left(-\frac{T_s}{2RC}\right)^2 \frac{1}{2!} + \ldots\right\}\right]$$

$$= V\left[\frac{T_s}{2RC} - \left(\frac{T_s}{RC}\right)^2 \frac{1}{8}\right]$$

At $t = T_s$, $$v_o = V_s$$

$\therefore$ $$V_s = V(1 - e^{-T_s/RC})$$

$$= V\left[1 - \left\{1 - \frac{T_s}{RC} + \left(-\frac{T_s}{RC}\right)^2 \frac{1}{2!} + \ldots\right\}\right]$$

$$= V\left[\frac{T_s}{RC} - \frac{1}{2}\left(\frac{T_s}{RC}\right)^2\right]$$

The displacement error e_d is given by

$$e_d = \frac{(v_s - v_s')_{\max}}{V_s} = \frac{V\left[\frac{T_s}{2RC} - \frac{1}{8}\frac{T_s^2}{(RC)^2}\right] - \frac{V}{2}\left[\frac{T_s}{RC} - \frac{T_s^2}{2(RC)^2}\right]}{V\left[\frac{T_s}{RC} - \left(\frac{T_s}{RC}\right)^2 \frac{1}{2}\right]}$$

$$= \frac{\frac{V}{2}\left[-\frac{T_s^2}{4(RC)^2} + \frac{T_s^2}{2(RC)^2}\right]}{V\left[\frac{T_s}{RC}\right]}$$

$$= \frac{1}{2}\left[\frac{\frac{1}{4}\left(\frac{T_s}{RC}\right)^2}{\frac{T_s}{RC}}\right] = \frac{1}{8}\frac{T_s}{RC} = \frac{e_s}{8}$$

$\therefore$ $$e_d = \frac{e_s}{8}$$

This proves that $$e_d = \frac{e_s}{8} = \frac{e_t}{4} \quad \text{or} \quad e_s = 2e_t = 8e_d$$

If a capacitor *C* is charged by a constant current /, then the voltage across *C* is *ft/C*. Hence the rate of change of voltage with time is given by

Sweep speed = I/C

UNIJUNCTION TRANSISTOR

As the name implies a UJT has only one p-n junction, unlike a BJT which has two p-n junctions. It has a p-type emitter alloyed to a lightly doped n-type material as shown in Figure 5.4(a). There are two bases: base B| and base **B_2,** base B] being closer to the emitter than base B_2. The p-n junction is formed between the p-type emitter and n-type silicon slab.

Originally this device was named as double base diode but now it is commercially known as UJT. The equivalent circuit of the UJT is shown in Figure 5.4(b). /?$_B$] is the resistance between base B! and the emitter, and it is basically a variable resistance, its value being dependent upon the emitter current i'$_E$. /?$_{B2}$ is the resistance between base 62 and the emitter, and its value is fixed.

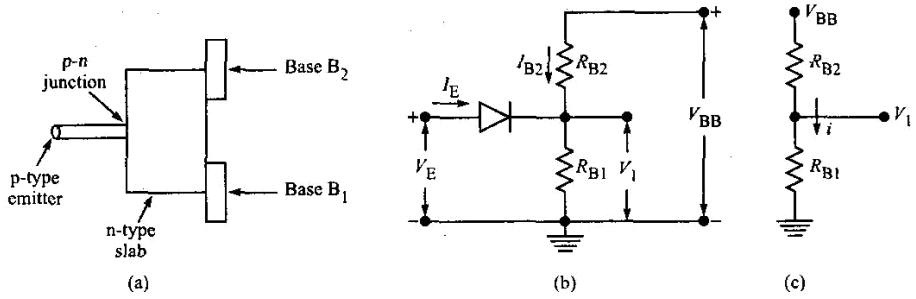


Figure 5.4 (a) Construction of UJT, (b) equivalent circuit of UJT, and (c) circuit when $i_E = 0$.

If IE = 0, due to the applied voltage V_{BB}, a current i results as shown in Figure 5.4(c).

$$i = \frac{V_{BB}}{R_{B1} + R_{B2}}$$

$$V_1 = iR_{B1} = \frac{V_{BB}}{R_{B1} + R_{B2}} R_{B1} = \frac{R_{B1}}{R_{B1} + R_{B2}} V_{BB}$$

The ratio $\frac{R_{B1}}{R_{B1} + R_{B2}}$ is termed the *intrinsic stand off ratio* and is denoted by η. Therefore,

$$\eta = \frac{R_{B1}}{R_{B1} + R_{B2}} \quad \text{when } i_E = 0.$$

$$V_1 = \eta V_{BB}$$

From the equivalent circuit, it is evident that the diode cannot conduct unless the emitter voltage

$$V_E = V_\gamma + V_1$$

where V_y is the cut-in voltage of the diode.

This value of emitter voltage which makes the diode conduct is termed *peak voltage* and is denoted by V_P.

$$V_P = V_\gamma + V_1$$

$$V_P = V_\gamma + \eta V_{BB} \quad \text{since } V_1 = \eta V_{BB}$$

It is obvious that if $V_E < V_P$, the UJT is OFF and if $V_E > V_P$, the UJT is ON.

The symbol of UJT is shown in Figure 5.5(a). The input characteristics of UJT (plot of VE versus /E) are shown in Figure 5.5(b). The main application of UJT is in switching circuits wherein rapid discharge of capacitors is very essential. UJT sweep circuit is called a relaxation oscillator.

SWEEP CIRCUIT USING UJT

Many devices are available to serve as the switch S. Figure 5.6(a) shows the exponential sweep circuit in which the UJT serves the purpose of the switch. In fact, any current-controlled negative-resistance device may be used to discharge the sweep capacitor.

The supply voltage V_{yY} and the charging resistor *R* must be selected such that the load line intersects the input characteristic in the negative-resistance region. Assume that the UJT is OFF. The capacitor *C* charges from V_YY through *R*. When it is charged to the peak value V_P, the UJT turns ON and the capacitor now discharges through the UJT. When the capacitor discharges to the valley voltage V_V» tne UJT turns OFF, and again the capacitor starts charging and the cycle repeats. The capacitor voltage appears as shown in Figure 5.6(b). The expression for the sweep time T_S can be obtained as follows.

For $0 < t < T_s$, $v_s = V_{YY} - (V_{YY} - V_V)\, e^{-t/RC}$

At $t = T_s$, $v_o = v_s = V_P$

$\therefore$ $V_P = V_{YY} - (V_{YY} - V_V)e^{-T_s/RC}$

i.e. $(V_{YY} - V_V)e^{-T_s/RC} = V_{YY} - V_P$

or $$e^{T_s/RC} = \frac{V_{YY} - V_V}{V_{YY} - V_P}$$

$\therefore$ $$T_s = RC \ln \frac{V_{YY} - V_V}{V_{YY} - V_P}$$

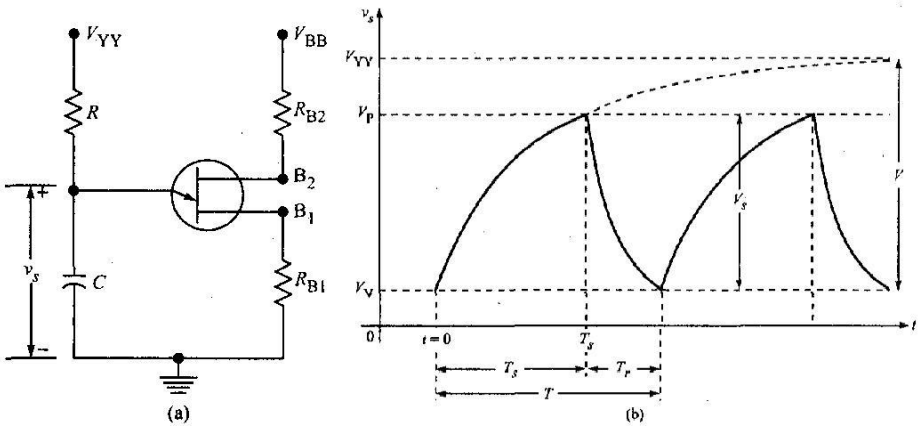


Figure 5.6 (a) UJT sweep circuit and (b) output waveform across the capacitor.

MILLER AND BOOTSTRAP TIME-BASE GENERATORS—BASIC PRINCIPLES

The linearity of the time-base waveforms may be improved by using circuits involving feedback. Figure 5.10(a) shows the basic exponential sweep circuit in which S opens to form the sweep. A linear sweep cannot be obtained from this circuit because as the capacitor charges, the charging current decreases and hence the rate at which the capacitor charges, i.e. the slope of the output waveform decreases. A

perfectly linear output can be obtained if the initial charging current / = *VIR* is maintained constant. This can be done by introducing an auxiliary variable generator v whose generated voltage v is always equal to and opposite to the voltage across the capacitor as shown in Figure 5.10(b). Two methods of simulating the fictitious generator are discussed below.

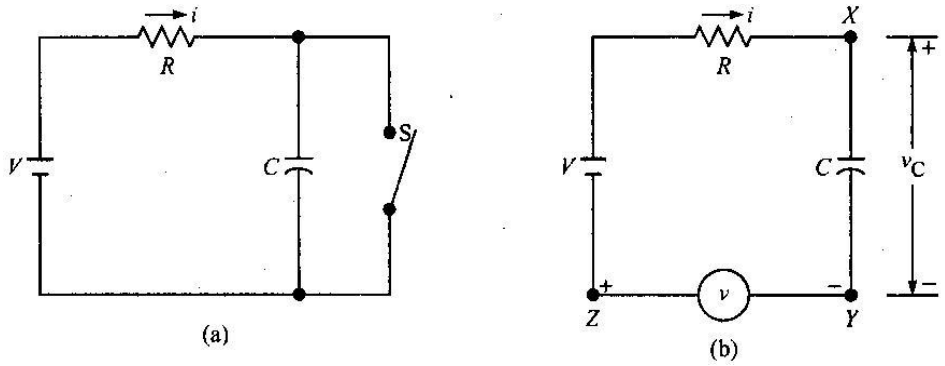


Figure 5.10 (a) The current decreases exponentially with time and (b) the current remains constant.

In the circuit of Figure 5.10(b) suppose the point Z is grounded as in Figure 5.11(a). A linear sweep will appear between the point Y and ground and will increase in the negative direction. Let us now replace the fictitious (imaginary) generator by an amplifier with output terminals YZ and input terminals XZ as shown in Figure 5.11(b). Since we have assumed that the generated voltage is always equal and opposite to the voltage across the capacitor,

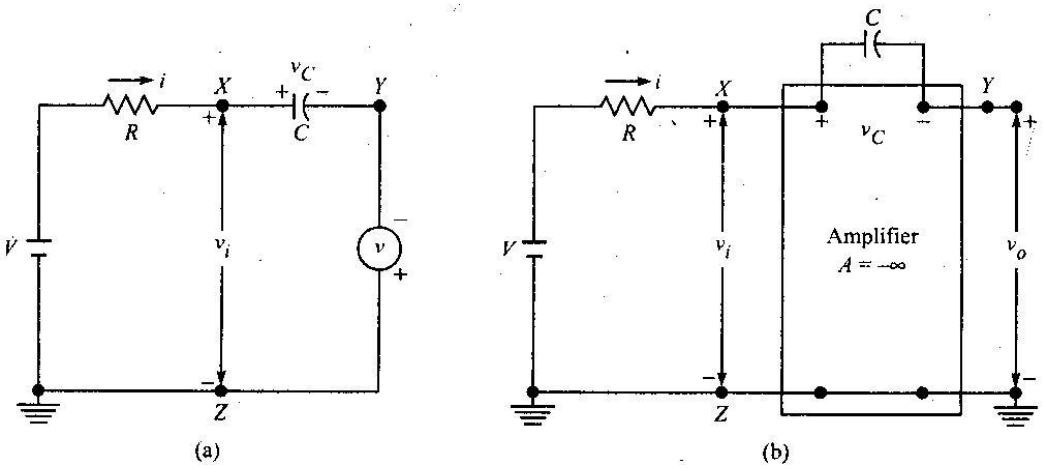


Figure 5.11 (a) Figure 5.10(b) with Z grounded and (b) Miller integrator circuit.

the voltage between X and Z is equal to zero. Hence the point X acts as a virtual ground. Now for the amplifier, the input is zero volts and the output is a finite negative value. This can be achieved by using an operational integrator with a gain of infinity. This is normally referred to as the Miller integrator circuit or the Miller sweep.

Suppose that the point Y in Figure 5.10(b) is grounded and the output is taken at Z. A linear sweep will appear between Z and ground and will increase in the positive direction. Let us now replace the fictitious generator by an amplifier with input terminals XY and output terminals ZY as shown in Figure 5.12. Since we have assumed that the generated voltage v at any instant is equal to the voltage across the

capacitor vc, then v_0 must be equal to v,-, and the amplifier voltage gain must be equal to unity. The circuit of Figure 5.12 is referred to as the Bootstrap sweep circuit.

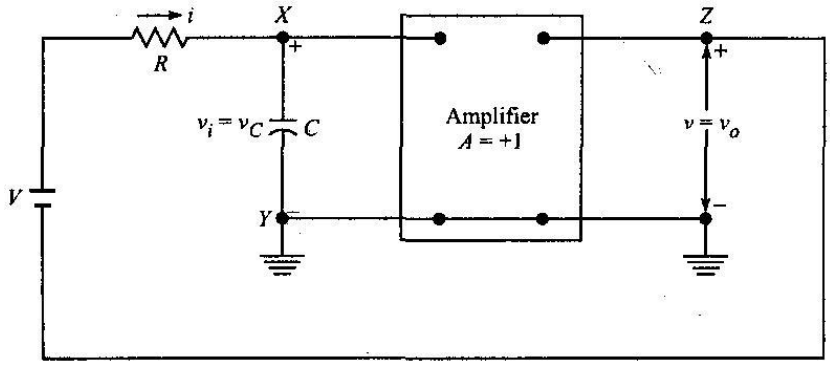


Figure 5.12 Bootstrap sweep circuit.

The Miller sweep

The Miller integrating circuit of Figure 5.11(b) is redrawn in Figure 5.13(a). A switch S at the closing of which the sweep starts is included. The basic amplifier has been replaced at the input side by its input resistance and on the output side by its Thevenin's equivalent. R_0 is the output resistance of the amplifier and A its open circuit voltage gain. Figure 5.13(b) is obtained by replacing V, R and tf, on the input side by a voltage source V in series with a resistance R' where

$$V' = V\frac{R_i}{R_i + R} = \frac{V}{1 + \frac{R}{R_i}} \quad \text{and} \quad R' = R \| R_i = \frac{RR_i}{R + R_i}$$

Neglecting the output resistance in the circuit of Figure 5.13{b), if the switch is closed at $t = 0$ and if the initial voltage across the capacitor is zero, then v_0 (f = 0^+) = 0, because at / = 0~, V; ~ 0 and since the voltage across the capacitor cannot change instantaneously.

$$\text{At } t = 0^+, \qquad v_i - Av_i = 0 \qquad \text{or} \qquad v_i = Av_i = v_o = 0$$

This indicates that the sweep starts from zero.

At $t = \infty$, the capacitor acts as an open-circuit for dc. So no current flows and therefore

$$v_i = V' \qquad \text{and} \qquad v_o = AV'$$

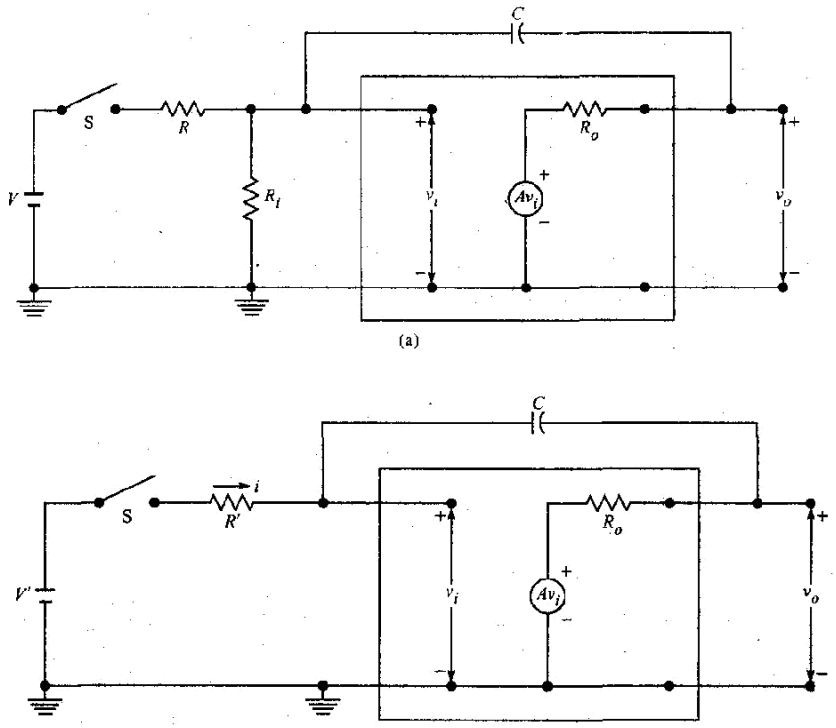


Figure 5.13 (a) A Miller integrator with switch S, input resistance R_f and Thevenin's equivalent on the output side and (b) Figure 5.13(a) with input replaced by Thevenin's equivalent.

This indicates that the output is exponential and the sweep is negative-going since A is a negative number.

$$\text{Slope error, } e_s = \frac{V_s}{V}$$

where V_S is the sweep amplitude and V is the peak-to-peak value of the output.

$$e_s(\text{miller}) = \frac{V_s}{|A|V'} = \frac{V_s}{|A|} \cdot \frac{R_i + R}{VR_i} = \frac{V_s}{V} \cdot \frac{1 + \dfrac{R}{R_i}}{|A|}$$

$$\frac{1 + \dfrac{R}{R_i}}{|A|}$$

The deviation from linearity is times that of an RC circuit charging directly from a source V.

If R_0 is taken into account, the final value attained by v_0 remains as before, $AV = - |A|V$. The initial value however is slightly different.

To find v_0 at $t = 0^+$, writing the KVL around the mesh in Figure 5.13(b), assuming zero voltage across the capacitor, we have

$$V' - R'i - R_o i - Av_i = 0$$

$$v_i = V' - R'i$$

From the above equations, we find

$$v_i(t = 0^+) = \Delta v_i = v_o(t = 0^+) = \Delta v_o = \frac{\left(\frac{R_o}{R'}\right)V'}{1 - A + \frac{R_o}{R'}}$$

$$v_i(t = 0^+) \approx \frac{R_o V'}{R'|A|}$$

Therefore, if R_0 is taken into account, $v_0(t = 0^+)$ is a small positive value and still it will be a negative-going sweep with the same terminal value. Thus the negative-going ramp is preceded by a small positive jump. Usually this jump is/small compared to the excursion AV', Hence, improvement in linearity because of the increase in total excursion is negligible.

The bootstrap sweep

Figure 5.14 shows the bootstrap circuit of Figure 5.12. The switch S at the opening of which the sweep starts is in parallel with the capacitor *C.* Here, /?,- is the input resistance, *A* is the open-circuit voltage gain, and R_0 is the output resistance of the amplifier.

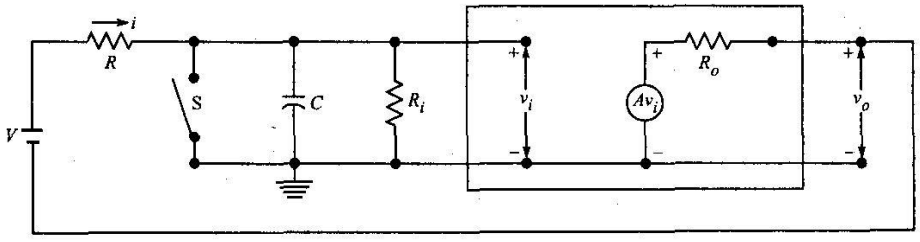


Figure 5.14 Bootstrap circuit of Figure 5.12 with switch S which opens at (= 0, input resistance R_f, and Thevenin's equivalent of the amplifier on the output side.

At t = 0~, the switch was closed and so v_t - 0, Since the voltage across the capacitor cannot change instantaneously, at t = 0* also, v(- = 0 and hence Av, = 0, and the circuit shown in Figure 5.15 results.

$$t = 0^+, \qquad v_o = -V\frac{R_o}{R + R_o}$$

The output has the same value at t = 0 and hence there is no jump in the output voltage at t = 0.

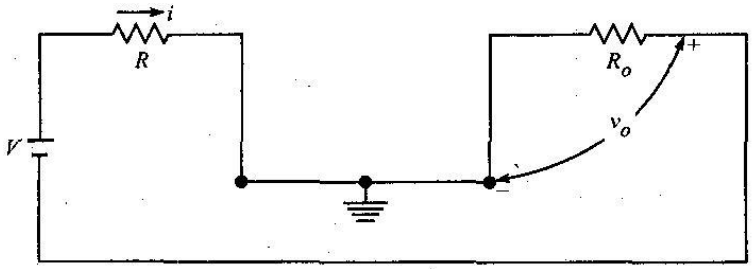


Figure 5.15 Equivalent circuit of Figure 5.14 aU = 0.

At t = <*>, the capacitor acts as an open-circuit and the equivalent circuit shown in Figure 5.16 results.

$$v_o(t=\infty) = AV_i - iR_o = AiR_i - iR_o = i(AR_i - R_o)$$

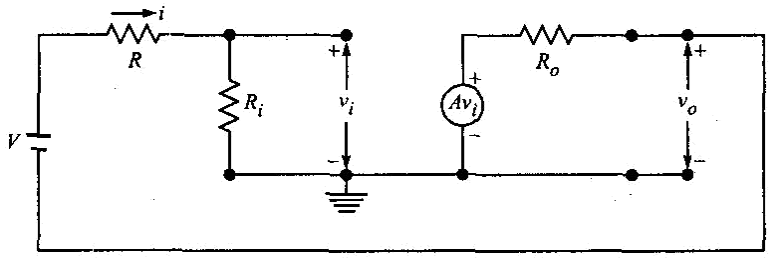


Figure 5.16 Equivalent circuit of Figure 5.14 at $t = \infty$.

Writing KVL in the circuit of Figure 5.16,

$$V - iR - iR_i + AV_i - iR_o = 0$$

i.e.
$$i = \frac{V}{R + R_o + R_i(1 - A)}$$

$\therefore$
$$v_o(t=\infty) = \frac{V(AR_i - R_o)}{R + R_o + R_i(1 - A)}$$

Since A « 1, and if R_0 is neglected, we get

$$v_o(t=\infty) = \frac{V}{(1 - A) + \frac{R}{R_i}}$$

Since R_0 « /?, v_0 at t = 0 can be neglected compared to the value of v_0 at t - <». Then the total excursion of the output is given by

$$v_o(t=\infty) - v_o(t=0) = \frac{V}{(1 - A) + \frac{R}{R_i}}$$

and the slope error is

$$e_s(\text{bootstrap}) = \frac{\text{Sweep amplitude}}{\text{Total excursion of output}} = \frac{V_s}{V\left[(1 - A) + \frac{R}{R_i}\right]} = \frac{V_s}{V}\left(1 - A + \frac{R}{R_i}\right)$$

This shows that the slope error is [1 - A + (R/Rj)] times the slope error that would result if the capacitor is charged directly from V through a resistor.

Comparing the expressions for the slope error of Miller and bootstrap circuits, we can see that it is more important to keep R/Rj small in the bootstrap circuit than in the Miller circuit. Therefore, the

Miller integrator has some advantage over the bootstrap circuit in that in the Miller circuit a higher input impedance is less important.

THE TRANSISTOR MILLER TIME-BASE GENERATOR

Figure 5.17 shows the circuit diagram of a transistor Miller time-base generator. It consists of a three-stage amplifier. To have better linearity, it is essential that a high input impedance amplifier be used for the Miller integrator circuit. Hence the first stage of the amplifier of Figure 5.17 is an emitter follower. The second stage is a common-emitter amplifier and it provides the necessary voltage amplification. The third stage (output stage) is also an emitter follower for two reasons. First, because of its low output impedance R_0 it can drive a load such as the horizontal amplifier. Second, because of its high input

impedance it does not load the collector circuit of the second stage and hence the gain of the second stage can be very high. The capacitor C placed between the base of Qi and the emitter of Q_3 is the timing capacitor. The sweep speed is changed from range to range by switching *R* and *C* and may be varied continuously by varying V_{BB}.

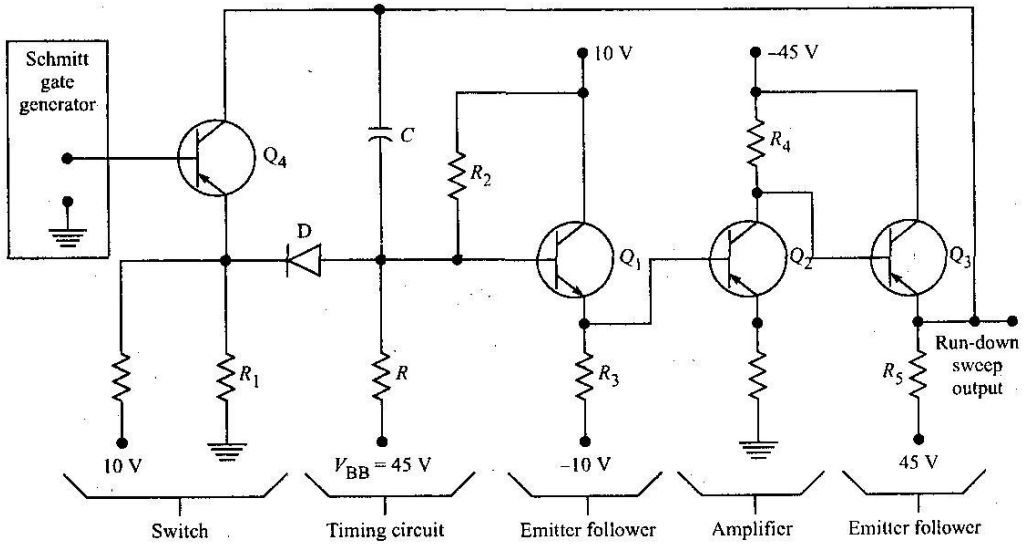


Figure 5.17 A transistorized Miller time-base generator.

Under quiescent condition, the output of the Schmitt gate is at its lower level. So transistor Q_4 is ON. The emitter current of Q_4 flows through *RI* and hence the emitter is at a negative potential. Therefore the diode D conducts. The current through *R* flows through the diode D and the transistor Q_4. The capacitor *C* is bypassed and hence is prevented from charging. When a triggering signal is applied, the output of the Schmitt gate goes to its higher level. So the base voltage of Q_4 rises and hence the transistor Q_4 goes OFF. A current flows now from 10 V source through *RI*. The positive voltage at the emitter of Q_4 now

makes the diode D reverse biased. At this time the upper terminal of *C* is connected to the collector of Q_4 which is in cut-off. The capacitor gets charged from V_{BB} and hence a run down sweep output is obtained at the emitter of Q_3. At the end of the sweep, the capacitor *C* discharges rapidly through D and Q_4. Considering the effect of the capacitance *C*\, the slope or sweep speed error is given by

$$e_s = \frac{V_s}{V}\left(1 - A + \frac{R}{R_i} + \frac{C}{C_1}\right)$$

THE TRANSISTOR BOOTSTRAP TIME-BASE GENERATOR

Figure 5.18 shows a transistor bootstrap time-base generator. The input to transistor Q] is the gating waveform from a monostable multivibrator (it could be a repetitive waveform like a square wave). Figure 5.19(a) shows the base voltage of Qj. Figure 5.19(b) shows the collector current waveform of Qj and Figure 5.19(c) shows the output voltage waveform at the emitter of q_2

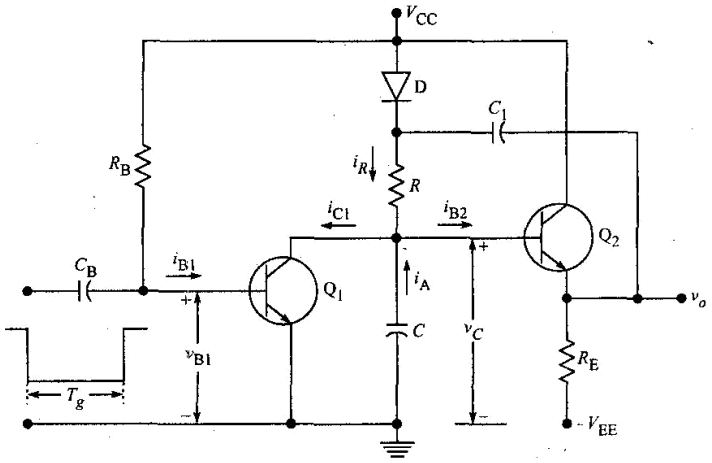


Figure 5.18 A voltage time-base generator.

Quiescent conditions

Under quiescent conditions, i.e. before the application of the gating waveform at *t* - 0, Q| is in saturation because it gets enough base drive from *YCC* through ^B- So the voltage across the capacitor which is also the voltage at the collector of Qj and the base of Q2 is VCE (sat). Since Q_2 is conducting and acting as an emitter follower, the voltage at the emitter of Q_2 which is also the output voltage is less than this base

voltage by V_{BE2}, i.e. $v_o = V_{CE}(sat) - V_{BE2}$

is a small negative voltage (a few tenths of a volt negative). If we neglect this small voltage as well as the small drop across the diode D, then the voltage across *C*\ as well as across *R* is Vcc-Hence the current i> through *R* i§ *Vcc/R*- Since the quiescent output voltage at the emitter of Q_2 is close to zero, the emitter

current of Q_2 is $V_{EE}/J?_E$. Hence the base current of Q_2 is $i_{B2} = V_{EE}$ /

h_{FE} R_E $i_R = i_{C1} + i_{B2}$

Since the base current of Q_2, i.e. $/_{B2}$ is very small compared with the collector current i_{C1} of Q_1

$$i_{C1} \approx i_R \approx \frac{V_{CC}}{R}$$

For Qj to be really in saturation under quiescent condition, its base current (($_B$i = V_{CC}/R_B) t be at least equal to I'CI#*FE> i.e. V_CC//IFE^. so that

$$\frac{V_{CC}}{R_B} > \frac{V_{CC}}{h_{FE}R} \qquad \text{i.e.} \qquad R_B < h_{FE}R$$

Formation of sweep

When the negative-going gating waveform is applied at t - 0, the transistor Q] is driven OFF. The current $/_C$i now flows into the capacitor C and so the voltage across the capacitor rises according to the equation

$$v_C = \frac{1}{C}\int i_{C1}\,dt = \frac{1}{C}\int \frac{V_{CC}}{R}\,dt = \frac{V_{CC}t}{RC}$$

$$v_o = v_C = \frac{V_{CC}t}{RC}$$

Assuming unity gain for the emitter follower,

Since the voltage across $C\backslash$ is constant and equal to VGO when the sweep starts, the diode is reverse biased and the current through R is supplied by the capacitor $C\backslash$.

The equation, $v_0 \sim V_{cc}t/RC$ is valid only if the gate duration T_g is small enough so that the calculated value of v_0 does not exceed Vcc- From Figure 5.18 it can be seen that when v_0 approaches VCG, the voltage VCE of Q2 approaches zero and the transistor Q_2 goes into saturation. Then it no longer acts as an emitter follower. Hence v_0 (also v_c) remains constant at V_{cc}. The current Vcc/K through Ci and R now flows from base to emitter of Q_2.

If the output v_0 reaches the voltage Vcc ^{m} a time $T_s < T_g$, then $V_{cc} = V_{cc}$ T_S / RC or T_S = RC

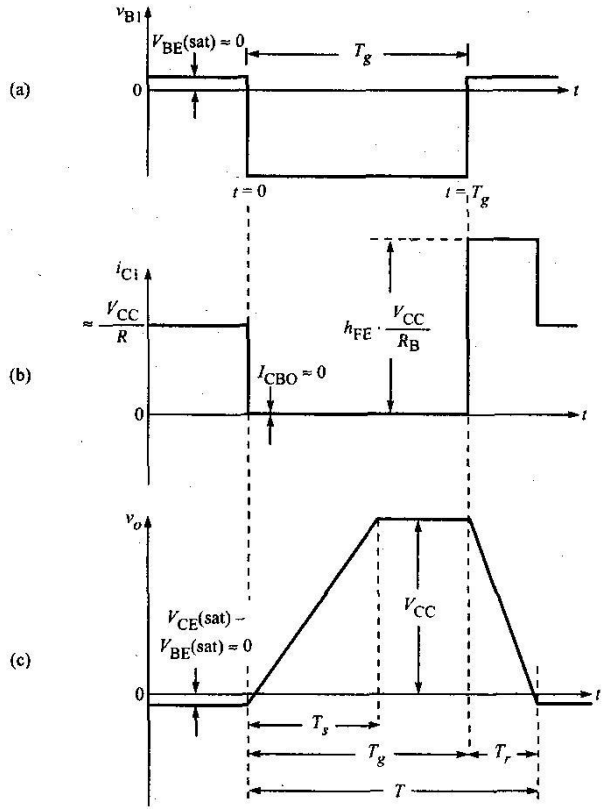


Figure 5.19 Voltage time-base generator of Figure 5.18: (a) the base voltage of $Q_{1\%}$ (b) the collector current of Qi, and (c) the output voltage at the emitter of Q2-

whereas if the sweep amplitude V_S is less than Vcc> then the maximum ramp voltage is given by

$$V_s = \frac{V_{CC} T_g}{RC}$$

Retrace interval

At $t = T_g$, when the gate terminates, the transistor Qi goes into conduction and a current $r'_{B}i = VCC/R\text{-}Q$ flows into the base of Qi. Hence a current/ci =/IFE*BI flows into the collector of Qj. This current remains constant till the transistor goes into saturation. Since Q] is ON the capacitor C discharges through Qi. Because of emitter follower action, when v_C falls, v_0 also falls by the same amount and so the voltage across R remains constant at V_{CC}. The constant current i_R = Vcc/R also flows through Qi. Applying KVL at the collector of Qi and neglecting $/_{B2}$,

$$i_{C1} = i_R + i_A \qquad \text{i.e.} \qquad i_A = i_{C1} - i_R = \frac{V_{CC}}{R_B} h_{FE} - \frac{V_{CC}}{R}$$

Since the discharging current of C, i.e. IA is constant, the voltage across *C* and hence the output voltage falls linearly to its initial value.

If the retrace time is T_r, then the charge lost by the capacitor = $I_A T_r$

$$\frac{i_A T_r}{C} = V_s$$

where V_S is the sweep amplitude. That is,

$$T_r = \frac{CV_s}{i_A} = \frac{C\frac{V_s}{V_{CC}}}{\frac{h_{FE}}{R_B} - \frac{1}{R}}$$

After *C* is discharged, the collector current is now supplied completely through *R* and becomes established at the value *V^c/R-* The retrace time can be reduced by choosing a small value of R_S. However if R_R is reduced greatly, then the collector current dissipation may be excessive.

$$i_C = h_{FE}\frac{V_{CC}}{R_B}$$

The recovery process

During the entire interval $T = T_g + T_r$ the capacitor C[discharges at a constant rate because the

Current $i = V_{CC}/R$ through it has remained constant. So it would have lost a charge $= \frac{V_{CC}}{R} T.$

Hence at the time *T* when the voltage across C and at the base of Q_2 returns to its value for $t < 0$, the voltage across Ci is smaller than it was at the beginning of the sweep. The diode D starts conducting at *t* - *T,* and the end of Ci, which is connected to D, returns to its initial voltage, i.e. Vcc- Therefore,.the other terminal of Ci which is connected to the emitter of Ch is at a more positive potential than it was at $t = 0$ and so Q_2 goes to cut-off. So the capacitor Ci charges through the resistor R_E with a current,

$i_E = V_{EE}/R_E.$

The maximum recovery time *T* for *C* can be calculated as follows.

$$\frac{V_{CC}}{R} T.$$

Charge lost by capacitor Ci in time *T* is

$$\frac{V_{EE}}{R_E} T_1.$$

Charge gained by capacitor Ci in minimum recovery time *T*

is

$$\frac{V_{CC}}{R} T = \frac{V_{EE}}{R_E} T_1$$

$$T_1 = \frac{V_{CC}}{V_{EE}} \frac{R_E}{R} T$$

This shows that $T\backslash$ is independent of $C\backslash$ and varies inversely with V_{EE}. $T\backslash$ can be reduced by increasing V_{EE}. However this modification will increase the quiescent current in Q_2 and hence its dissipation.

CURRENT TIME-BASE GENERATORS

We have mentioned earlier that a linear current time-base generator is one that provides an output current waveform a portion of which exhibits a linear variation with respect to time. This linearly varying current waveform can be generated by applying a linearly varying voltage waveform generated by a voltage time-base generator, across a resistor. Alternatively, a linearly varying current waveform can be generated by applying a constant voltage across an inductor. Linearly varying currents are required for magnetic deflection applications.

A SIMPLE CURRENT SWEEP

Figure 5.26(a) shows a simple transistor current sweep circuit. Here the transistor is used as a switch and the inductor L in series with the transistor is bridged across the supply voltage. R_d represents the sum of the diode forward resistance and the damping resistance. The gating waveform shown in Figure 5.26(b) applied to the base of the transistor is in two levels. These levels are selected such that when the input, is at the lower level the transistor is cut-off and when it is at the upper level the transistor Is in saturation. For $t < 0$, the input to the base is at its lower level (negative). So the transistor is cut-off. Hence no currents flow in the transistor and $i_L = 0$ and v_{CE} = Vcc- At f = 0, the gate signal goes to its upper level (positive). So the transistor conducts and goes into saturation. Hence the collector voltage falls to v_{CE}(sat) and the entire supply voltage V_{cc} is applied across the inductor. So the current through the inductor

$$i_L = \frac{1}{L} \int V_{CC}\, dt = \frac{V_{CC} t}{L}$$

increases linearly with time. This continues till $t = T_g$, at which time the gating signal comes to its lower level and so the transistor will be cut-off. During the sweep interval T_s (i.e. from $t = 0$ to $t = T_g$), the diode D is reverse biased and hence it does not conduct. At $t \sim T_s$, when the transistor is cut-off and no current flows through it, since the current through the inductor cannot change instantaneously it flows through the diode and the diode conducts. Hence there will be a voltage drop of $l_L R_d$ across the resistance R_d. So at $t = T_g$, the potential at the collector terminal rises abruptly to Vcc + *fiftd** i-^{e}- there is a voltage spike at the collector at $t = T_g$. The duration of the spike depends on the inductance of Z-^but

the amplitude of the spike does not. For $t > T_g$, the inductor current decays exponentially to zero with a time constant T- LIR_d. So the voltage at the collector also decays exponentially and settles at Vcc under steady-state conditions. The inductance L normally represents a physical yoke and its resistance R_L may not be negligible. If R_{CS} represents the collector saturation resistance of the transistor, the current increases in accordance with the equation

$$i_L = \frac{V_{CC}}{R_L + R_{CS}}(1 - e^{-(R_L+R_{CS})t/L})$$

$$\approx \frac{V_{CC}}{R_L + R_{CS}}\left(1 - \left\{1 - \frac{(R_L + R_{CS})t}{L} + \frac{1}{2}\left(-\frac{(R_L + R_{CS})t}{L}\right)^2\right\} + \dots\right)$$

$$= \frac{V_{CC}t}{L}\left(1 - \frac{1}{2}\frac{(R_L + R_{CS})t}{L}\right)$$

If the current increases linearly to a maximum value I_L, the slope error is given by

$$e_s = \frac{I_L}{\frac{V_{CC}}{R_L + R_{CS}}} = \frac{(R_L + R_{CS})I_L}{V_{CC}}$$

The inductor current waveform and the waveform at the collector of the transistor are shown in Figures 5.26(c) and 5.26(d) respectively. To maintain linearity, the voltage $(R_L$ + /?csXt across the total circuit resistance must be kept small compared with the supply voltage V_{CC}.

A TRANSISTOR CURRENT TIME-BASE GENERATOR

Figure 5.30 shows the circuit diagram of a transistor current time-base generator. Transistor Q! is a switch which serves the function of S in Figure 5.29. Transistor Qi gets enough base drive from V_{CC1} through KB $^{a\circ}$d hence is in saturation under quiescent conditions. At / = 0, when the gating signal is applied it turns off Qi and a trapezoidal voltage waveform appears at the base of Q_2. Transistors Q_2 and Q_3 are connected as darlington pair to increase the input impedance so that the trapezoidal waveform source is not loaded. Such loading would cause nonlinearity in the ramp part of the trapezoid.

The emitter resistor R_E introduces negative current feedback into the output stage and thereby improves the linearity with which the collector current responds to the base voltage. For best linearity it is necessary to make the emitter resistance as large as possible. R_E is selected so that the voltage developed across it will be comparable to the supply voltage

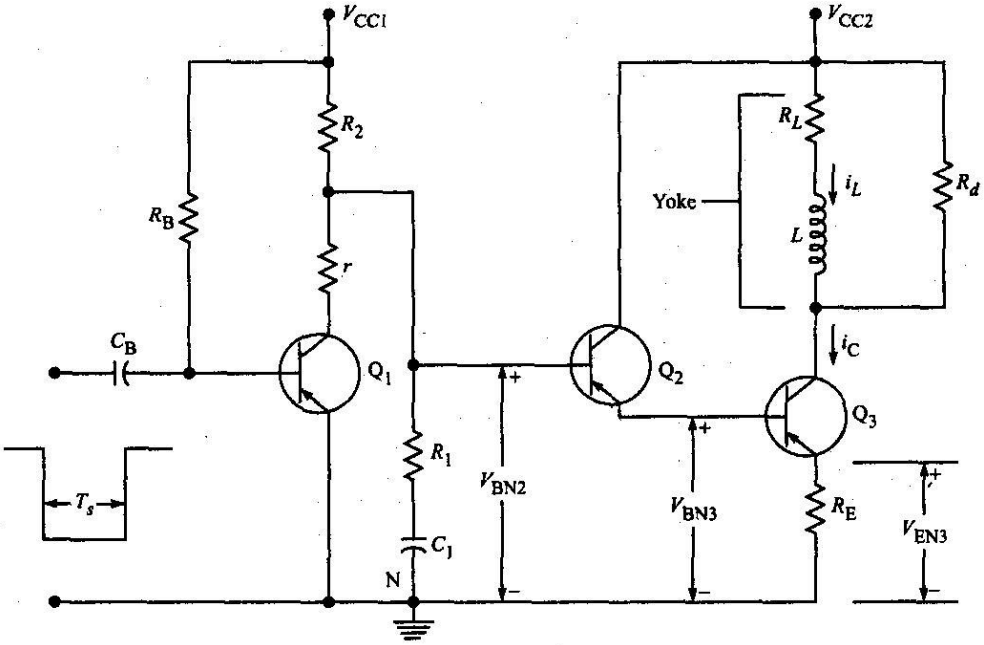


Figure 5.30 A transistor current sweep circuit.

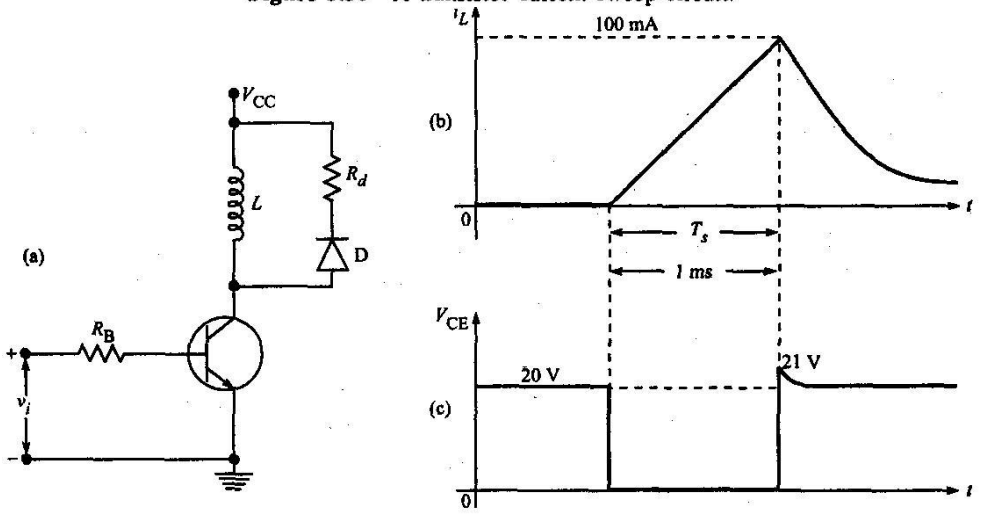


Figure 5.31 Example 5.15: (a) circuit diagram, (b) waveform of i_L, and (c) waveform of v_{CE}.

UNIT – V

SAMPLING GATES AND LOGIC GATES

IC families:

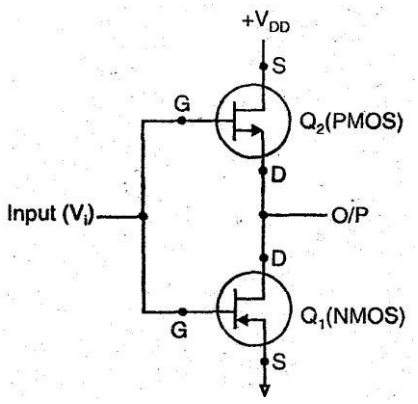
comparison of the important characteristics of various IC logic families.

	Parameter	RTL	I^2L	DTL	HTL	TTL	ECL	MOS	CMOS
1.	Basic Gate	NOR	NOR	NAND	NAND	NAND	OR-NOR	NAND	NOR or NAND
2.	Fan-out	5	Depends on injector current	8	10	10 to 20	25	20	20 to 50
3.	Power dissip-ation in mW	12	6mm to 70 μM	8-12	55	10	40-55	0.2-10	0.0025
4.	Noise immunity	Nominal	Poor	Good	Excellent	Very Good	Poor	Good	Very Good
5.	Propagation delay (in sec.)	12	25-250	30	90	10	0.75	300	70.0
6.	Clock rate (MHZ)	8	–	72	4	35	>60	2	10
7.	Available functions	High	LSI only	Fairly high	Nominal	Very high	High	low	High

(i) CMOS inverter

(ii) Tristate logic

(i) CMOS Inverter: It is complementary MOSFET obtained by using P-channel MOSPET and n-channel MOSFET simultaneously. The P and N channel are connected in series, their drains are connected together, output is taken from common drain point. Input is applied at common gate terminal. CMOS is very fast and consumes less power.



Case 1. When input Vi = 0. The V_{GS} (Gate source) voltage of Q1 will be 0 volt, it will be off. But Q2 will be ON; Hence output will be equal to +VDD or logic 1.

Case 2. When input Vi = 1, The V_{GS} (Gate source) voltage of Q2 will be 0 volt, it will be OFF, But Q1 will be ON. Hence output will be connected to•
ground or logic 0.
In this way, CMOS function as an inverter.

(ii) Tri-state logic: When there are three states i.e. state 0, state 1 and high impendence i.e. called Tri-state logic. High impedance is considered as state when no current pass through circuit. Although in state 0 and state 1 circuit functions and current flows through it.

- Propagation delay is the average transition delay time for a pulse to propagate from input to output of a switching circuit.
- Fan-in is the number of inputs to the gate which it can handle.
- Fan-out is the number of loads the output of a gate can drive without effecting its operation.
- Power dissipation is the supply voltage required by the gate to operate with 50% duty cycle at a given frequency
- RTL, DTL, DTL are the logic families which are now obsolete.
- TTL is the most widely used logic family.
- TTL gates may be:
  (a) Totem pole
  (b) Open collector
  (c) Tri-state .
- TTL is used in SSI and MSI Integrated circuits and is the fastest of all standard logic families.
- Totem pole TTL has the advantage of high speed and low power dissipation but its disadvantage is that it cannot be wired ANDed because of current spikes generation.
- Tri-state has three states : .
  (a) High

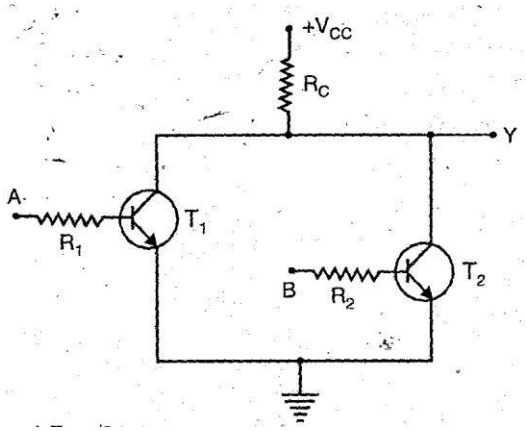
(b) Low

(c) High Impedance

- ECL is the fastest of all logic families because its propagation delay is very small i.e. of about 2 nsec.
- ECL can be wired ORed.
- MOS logic is the simplest to fabricate.
- MOS transistor can be connected as a resistor.
- MOSFET circuitry are normally constructed from NMOS devices because they are 3 times faster than PMOS devices.
- CMOS uses both P-MOS and N-MOS.
- CMOS needs less power as compared to ECL as they need maximum power.
- Both NMOS and PMOS are more economical than CMOS because of their greater packing densities.
- Speed of CMOS gates increases with increase in VDD.
- CMOS has large fan-out because of its low output resistance.

Schematic of RTL NOR gate and explain its operation.

RTL was the first to introduced. RTL NOR gate is as shown in fig.



Working:

Case I: When A = B = 0.

Both T1 and T2 transistors are in cut off state because the voltage is insufficient to drive the transistors i.e. VBE < 0.6 V: Thus, output Y will be high, approximately equal to supply voltage Vcc. As no current flows through Rc and drop across Rc is also zero.

Thus, Y = 1, when A = B = 0.

Case II : When A = 0 and B = 1 or A = 1 and B = 0.

The transistor whose input is high goes into saturation where as other will goes to off cut state. This positive input to transistor increases the voltage drop across the collector resistor and decreasing the positive output voltage.

Thus, Y = 0,when A= 0 and B = 1 or A = 1 and B = 0.

Case III : When A = B = 1**.** Both the transistors T1 and T2 goes into saturation and output voltage is equal to saturation voltage.

Thus, Y = 0,when A = B = 1

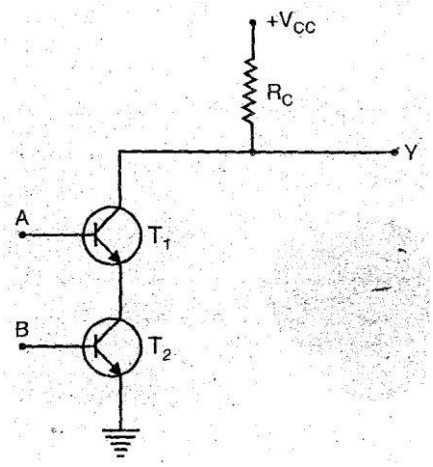
Truth Table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Which is the output of NOR gate.

DCTL NAND gate with the help of suitable circuit diagram.

DCTL NAND gate circuit diagram is as shown:



Working

Case I: When A = B = 0. Both transistors T1 and T2 goes to cut off state. As the voltage is not sufficient to drive the transistor into saturation. Thus, the output voltage equal to Vcc.

When A = B = 0, output Y = 1

Case II: When A = 0 and B = 1 or A = 1 and, B = 0. The corresponding transistor goes to cut off state and the output voltage equals to Vcc.

Thus, When A = 0 and B = 1 or A = 1 and B = 0, Output Y = 1.

Case III: When A = B = 1. Both transistors T1 and T2 goes into saturation state and output voltage is insufficient to consider as '1'

Thus when A B = 1, output Y = 0.

Truth Table

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Which is the output of NAND gate.

Compare standard TTL, Low power TTL and high speed TTL logic families.

Name of the Logic Family	Propagation Delay (ns)	Power Dissipation (mW)	Fan out	Max. Clock Rate (MHz)
1. Standard TTL	9	10	10	35
2. Low power TTL	33	1	20	3
3. High sped TTL	6	23	10	50

characteristics and specification of CMOS.

1 Power supply (VDD) = 3 — 15 Volts

2. Power dissipation (Pd) = 10 nW

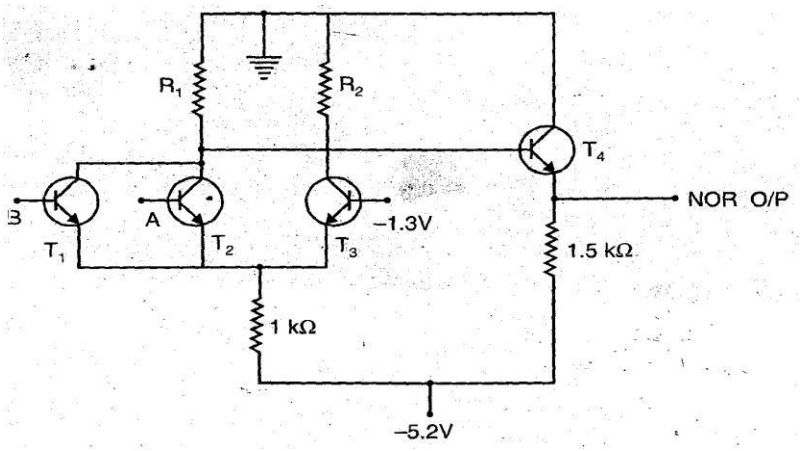
3. Propagation delay (td) = 25 ns

4. Noise margine (NM) = 45% of

VDD 5, Fan out (FO) = >50

Two input ECL NOR gate

The circuit diagram of two input ECL NOR gate is as shown:



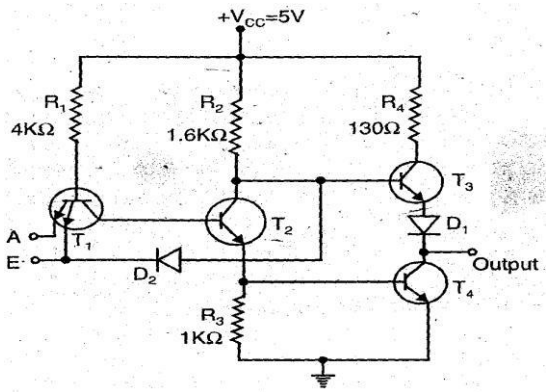
Working

Case I : When A = B = 0, the reference voltage of T3 is more forward biased then T1 and T2. Thus, T3 is ON and T1, T2 remains OFF. The value of R1 is such-that the output of NOR gate is high .i.e. '1'.

Case II: When A = 1 or B = 1 or A = B = 1, the corresponding transistors are ON, as they are more forward biased that T3 and thus T3 is OFF. Which makes the NOR output to be low i.e. '0'.

This shows that the circuit works as a NOR gate.

TTL inverter.



Tristate TTL inverter utilizer the high-speed operation of totem-pole arrangement while permitting outputs to be wired ANDed (connected together). It is called tristate TTL because it allows three possible output stages. HIGH, LOW and High-Impedance. We know that transistor T3 is ON when output is HIGH and T4 is ON when output is LOW. In the high impedance state both transistors, transistor T3 and T4 in the totem pole arrangement are med OFF. As a result the output is open or floating, it is neither LOW nor HIGH.

The above fig. shows the simplified tristate inverter. It has two inputs A and E. A is the normal logic input whereas E is an ENABLE input. When ENABLE input is HIGH, the circuit works as a normal inverter. Because when E is HIGH, the state-of the transistor T1 (either ON or OFF) depends on the logic input A and the additional component diode is open circuited as cathode is at logic HIGH. When ENABLE input is LOW, regardless of the state of logic input the base-emitter junction of T is forward biased and as a result it turns ON. This shunts the current through R1 away from T2 making it OFF. As T2 is OFF, there is no sufficient drive for T4 conduct and hence T4 turns OFF. The LOW at ENABLE input also forward biases diode D2, which shunt the current away from the base of T3, making it OFF. In this way, when ENABLE output is LOW, both transistors are OFF and output is at high impedance state.

ECL OR gate

ECL or gate : Emitter-coupled logic (ECL) is the fastest of all logic families and thus it is used in applications where very high speed is essential. High speeds have become possible in ECL because the transistors are used in difference amplifier configuration, in which they are never driven into saturation and thereby the storage time is eliminated. Here, rather than switching the transistors from ON to OFF and vice-versa, they are switched between cut-off and active regions. Propagation delays of less than 1 ns per gate have become possible in ECL.

Basically, ECL is realized using difference amplifier in which the emitters of the two transistors are connected and hence it referred to as emitter-coupled logic. A 3-input ECL gate is shown in Fig. (A) which has three parts. The middle part is the difference amplifier which performs the logic operation.

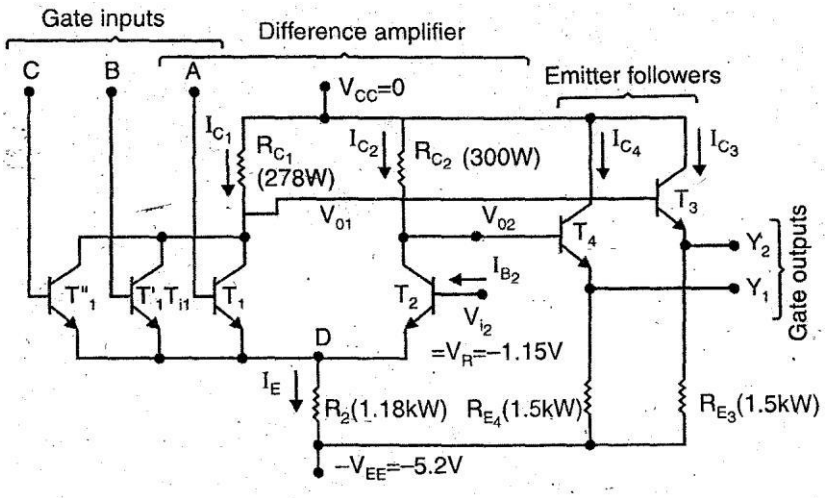


Fig. (A) A 3-input ECL OR/NOR Gate

Emitter followers are used for d.c. level shifting of the outputs, so that V (0) and V (1) are same for the inputs and the outputs. Note that two output Y1 and Y2 are available in this circuit which are complementary. Y1. corresponds to OR logic and Y2 to NOR logic and hence it is named as an OR/NOR gate.

Additional transistors are used in parallel to T1 to get the required fan-in. There is a fundamental difference between all other logic families (including MOS logic) and ECL as far as the supply voltage is concerned. In ECL, the positive end of the supply is connected to ground in contrast to other logic families in which negative end of the supply is grounded. This is done to minimize the effect of noise induced in the power supply and protection of the gate from an accidental short circuit developing between the output of a gate and ground. The voltage corresponding to V (0) and V (1) are both negative due to positive end of the supply being connected to ground. The symbol of an ECL OR/NOR gate is shown in Fig. (B)

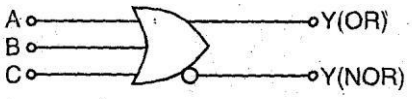
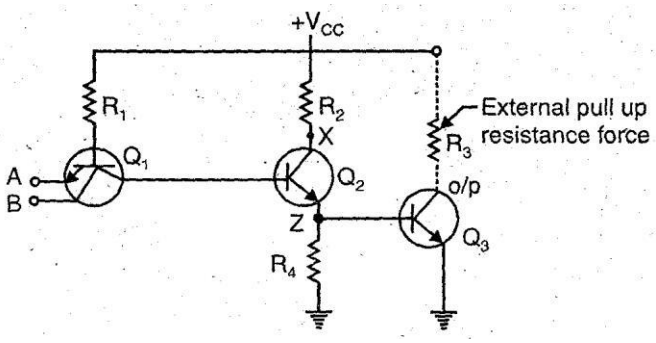


Fig. (B) The Symbol for a 3-input OR/NOR Gate

Open collector TTL NAND gate and explain its operation

The circuit diagram of 2-input NAND gate open-collector TTL gate is as shown:



Working:

Case.1 : When A = 0,B = 0

When both inputs A and B are low, both functions of Q1 are forward biased and Q2 remains off. So no current flows through R4 and Q3 is also off and its collector voltage is equal to Vcc i.e. Y = 1

Case2 : When A = 0, B = 1 and

Case 3: When A = 1, B = 0

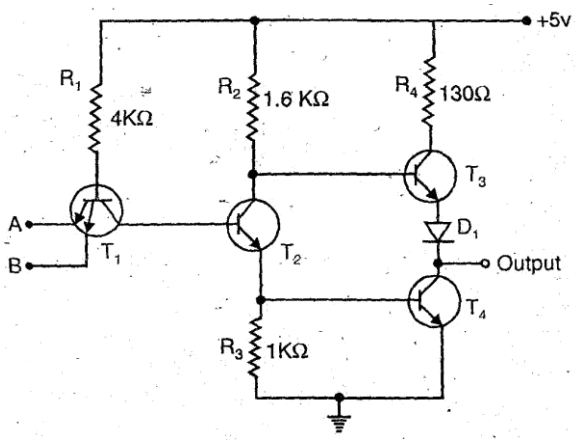
When one input is high and. other is low, then one junction is forward biased so Q2 is off and Q3 is also off. So collector voltage is equal to Vcc i.e. Y = 1

Case 4: When A = 1, B = 1

When both inputs are high, Q1 is turned off and Q2 turned 'ON' Q3 goes into saturation and hence Y = 0. The open-collector output has main advantage that wired ANDing is possible in it.

TTL NAND gate

Two input TTL NAND gate-is given in fig. (1). In this transistor T3 and T4 form a totem pole. Such type of configuration is called-as totem-pole output or active pull up output.



So, when A = 0 and B = 1 or (+5V). T1 conducts and T2 switch off. Since T2 is like an open switch, no current flows through it. But the current flows through the resistor R2 and into the base of transistor T3 to turn it ON. T4 remains OFF because there is no path through which it can receive base current. The output current flows through resistor R4 and diode D1. Thus, we get high' output.

When both inputs are high i.e. A = B = 1 or (+ 5V), T2 is ON and it drives T4 turning it ON. It is noted that the voltage at the base of T3 equals the sum of the base to emitter drop of

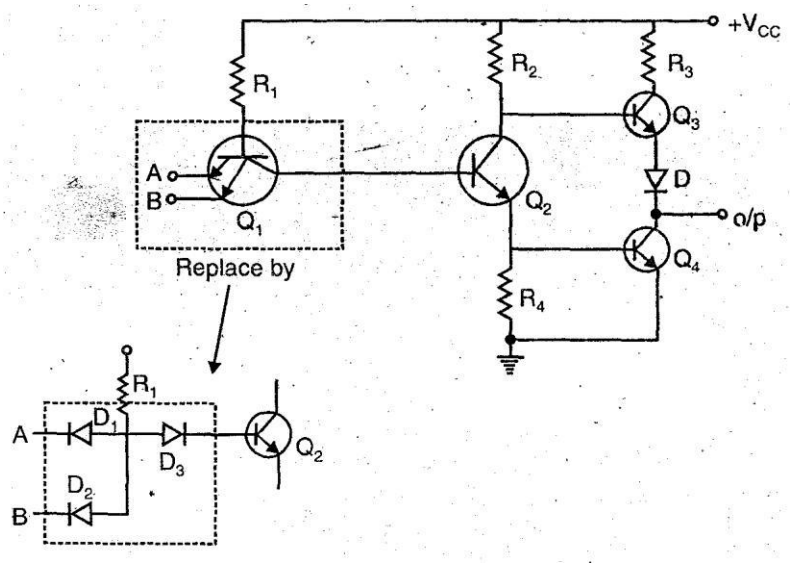
T4 and $V_{CE\ (Sat)}$ of T2.

The diode D1 does not allow base-emitter junction of T3 to be forward-biased and hence, T3 remains OFF when T4 is ON. Thus, we get low output.

It works as TTL NAND gate.

Totem pole NAND gate

In TTL Totem pole NAND gate, multiple emitter transistor as input is used. The no. of inputs may be from 2 to 8 emitters. The circuit diagram is as shown



Case 1:

When A = 0, B = 0

Now D1 and D2 both conduct, hence D3 will be off and make Q2 off. So its collector voltage rises and make Q3 'ON' and Q4 off; Hence output at Y = 1 (High)

Case 2 and Case 3:

If A = 0, B = 1 and A = 1, B=0

In both cases, the diode corresponding to low input will conduct and hence diode P3 will be OFF making Q2 OFF. In a similar way its collector voltage rises Q3 'ON' and Q4 'OFF'. Hence output voltage Y = 1 (High).

Case 4: A = 1, B = 1

Both diodes D1 and D2 will be off. D3 will be 'ON' and Q2 will 'ON' making Q4 also 'ON'.

But Q3 will be 'OFF'. So output voltage Y = 0.

All the four cases shows that circuit operates as a NAND gate.

Totem pole can’t be Wired ANDed due to current spike problem. The transistors used in circuits may get damaged over a period of time though not immediately. Sometimes voltage level rises high than the allowable.